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A NOVEL APPROACH OF IMPEDANCE SOURCE CASCADED MULTILEVEL INVERTER

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ABSTRACT: This paper deals with simulation of impedance source cascaded multilevel inverter. Impedance network in the cascaded multilevel inverter circuit will perform buck/boost operation. The use of Z-source inverter in industrial applications greatly increases its reliability by highly immune to EMI noises, improves power factor and reduces harmonic current and common- mode voltage. This impedance network reduces one stage(buck-boost) of power conversion system. Using impedance source multilevel inverter there is no problem of shoot through. This paper illustrate effective utilization of non – conventional resource(wind) which is used as source of one of the H bridge in cascaded multilevel inverter.

KEYWORDS: Z-source inverter ,Electromagnetic Interference(EMI) and cascaded multilevel inverter.

I.INTRODUCTION

In a traditional voltage-source inverter, the two switches of the same-phase leg can never be gated on at the same time because doing so would cause a short circuit (shoot through) to occur, which would destroy the inverter. In addition, the maximum output voltage obtainable can never exceed the dc bus voltage. Each converter generates a square wave voltage waveform with different duty ratios, which together form the output voltage waveform. These limitations can be overcome by the new Z-source inverter [1],[2]. In addition, the reliability of the inverter is greatly improved because the shoot through caused by electromagnetic interference (EMI) noise can no longer destroy the circuit. Thus, it provides a low-cost and reliable. Multilevel inverters synthesizing a large number of levels have a lot of merits such as improved output waveform, a smaller filter size, a lower EMI (Electro Magnetic Interference), and other advantages. The principle advantage of using multilevel inverters is the low harmonic distortion obtained due to the multiple voltage levels at the output and reduced stresses on the switching devices used. Due to their ability to synthesize waveforms with a better harmonic spectrum and attain higher voltages, multi-level inverters are receiving increasing attention in the past few years. The benefits are especially clear for medium-voltage drives in industrial applications [5],[6] and are being considered for future Naval ship propulsion systems.The multilevel inverter was introduced as a solution to increase the converter operating voltage above the voltage limits of classical semiconductors. Multilevel voltage source inverter (VSI) has been recognized as an important alternative to the normal two levels VSI, especially in high power application [4]. Using multilevel technique, the output voltage amplitude is increased, switching devices stress is reduced and the overall harmonics profile is improved. Several multilevel topologies are reported [1, 2, 3], and the most popular topology is Cascaded Multilevel Inverter (CMI). It offers several advantages compared to other topologies such as simple circuit layout, less components counts, modular in structure and avoid unbalance capacitor voltage problem. However as the number of output level increases, this topology becomes highly cumbersome because the number of power devices is increases.

II.IMPEDANCE NETWORK

The circuit diagram of impedance network is shown in the Fig. 1. It consists of a pair of capacitors and inductors respectively. The value of capacitors and inductors can be chosen based on the output voltage requirement. A diode is connected in the impedance network as shown Fig. 1 to block the reverse flow of current. A voltage type impedance source inverter can assume all active and null switching states of VSI. Unlike conventional VSI, a impedance source fed inverter has a unique feature of allowing both power switches of a phase leg to be turned ON simultaneously (shoot-through state) without damaging the inverter.

The impedance network changes the circuit configuration from that of a voltage source to an impedance source (i.e. Z-source). It allows the VSI to be operated in a new state called the shoot-through state in which the two switching devices in the same leg are simultaneously switched-on to effect short-circuit of the dc link [3]. During this state, energy is transferred from the capacitors to inductors, thereby giving rise to the voltage boost capability of the impedance source fed inverter.

The impact of the phase leg shoot-through on the inverter performance can be analyzed by considering the circuit diagram shown in Fig. 1.

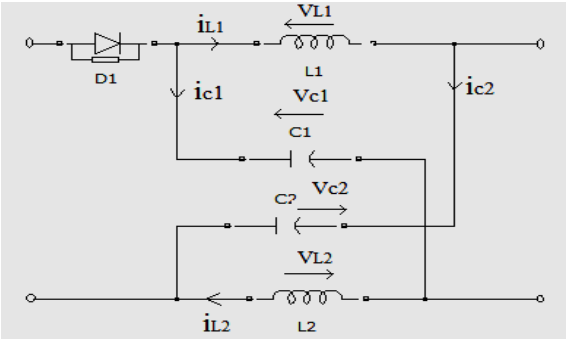

Fig. 1 Impedance network

When the impedance network is in non – shoot – through state unlike normal voltage source inverter it can assume a third distinct state for inductive voltage boosting by turning ON two switches from any phase-leg simultaneously to create a short-circuit across the inverter dc-link (vi = 0V). Doing so will not damage any semiconductor devices because the energy supplied by the dc source and shunt capacitors is prevented from surging instantaneously by the Z- source inductors. Therefore (assuming $L1 = L2 = L$ and $C1 = C2 = C$):

$$vL1 = vL2 = VL = VC1 = VC2 = VC \quad \ldots\ldots\ldots (1)$$

$$vL = vdc - VC \quad \ldots\ldots\ldots (2)$$

$$Vi = 2VC - vdc \quad \ldots\ldots\ldots (3)$$

III.IMPEDANCE SOURCE SEVEN LEVEL CASCADED MULTILEVEL INVERTER

Simulated configuration of impedance source seven level cascaded multilevel inverter is shown in Fig.2. It consists of twelve IGBT/Diode switches. Each H bridge consists of four switches respectively.

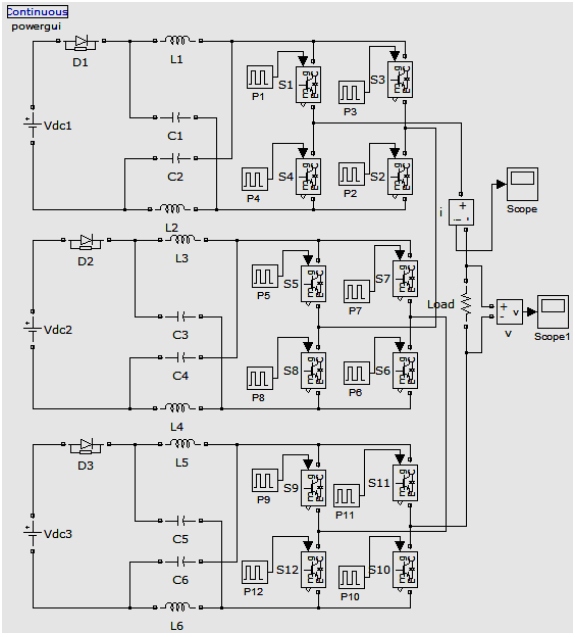

Fig. 2 Simulation diagram of impedance source Cascaded multilevel inverter

Source for each H bridge is fed from impedance network. This voltage will be less or greater than input dc voltage. Nature of the load is pure resistive. Based on the values of inductor pairs and capacitor pairs in a impedance network magnitude of Vdc is chosen. Since each H bridge in an inverter circuit can provide three voltage levels(zero, positive dc voltage and negative dc voltage). So switching state is defined for H bridge in an inverter circuit as shown in below table.

Table 1: switching states

SHi	SLi	SRi	Vgi	idci
-1	0	1	-vdci	-is
0	0	0	0	0
0	1	1	0	0
1	1	0	vdci	is

From above table, it can be seen that the general relationships for ith H bridge are

$$Vgi = (SLi - SRi)\, Vdci \quad \ldots\ldots\ldots (4)$$

$$idci = (SLi - SRi)\, is \quad \ldots\ldots\ldots (5)$$

Where,

SLi = Left arm switch in ith H bridge
SRi = Right arm switch in ith H bridge
SHi = Switching states for ith H bridge
Vgi = inverter output voltage for ith H bridge
Idci = Inverter dc current for ith H bridge
is = Source current

IV.WIND MODEL

Three phase permanent magnet synchronous generator is used in this proposed paper because of its advantages such as they do not require an additional DC supply for the excitation circuit, it avoids the use of slip rings, hence it is simpler and maintenance free and condensers are not required for maintaining the power factor in synchronous generators, as it is required in induction generator.

This permanent magnet synchronous generator output voltage is rectified using uncontrolled rectifier block and the ripples in the output is reduced by implementing the LC filter in a circuit. This filtered output is then connected as dc source of one of the H bridge in a impedance source cascaded multilevel inverter. This output voltage from permanent magnet synchronous generator is controlled by varying the preset model of synchronous generator and the wind speed.

In this paper wind model is implemented for first H bridge of impedance source seven level cascaded multilevel inverter as shown in Fig 3.

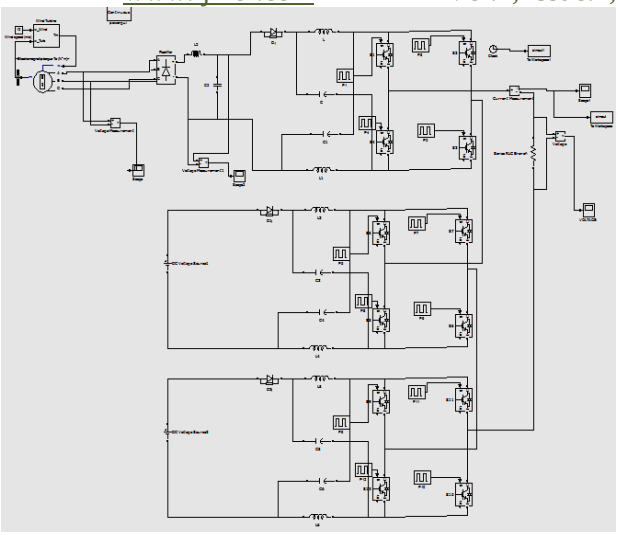

Fig. 3 Simulation diagram of impedance source Cascaded multilevel inverter with wind model

The output dc voltage from wind model is fed to the impedance network of first H bridge of impedance source cascaded multilevel inverter. This dc voltage from the rectifier block of wind model can be buck or boosted as based on requirement of the circuit.

Implemented wind model in impedance source cascaded multilevel inverter is shown in Fig.4

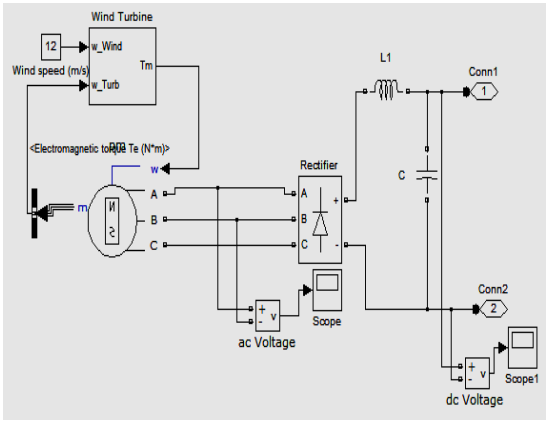

Fig.4. Simulation diagram of Wind model

V. RESULTS AND DISCUSSIONS

Experimental output voltage waveform for impedance source seven level cascaded multilevel inverter is shown in Fig. 5. Input dc voltage for second and third H bridge is given as 70V and for first H bridge 100V dc voltage will be supplied from the wind model. This 70V is boosted to 100V with the help of impedance network. This can be observed in below output voltage waveform.

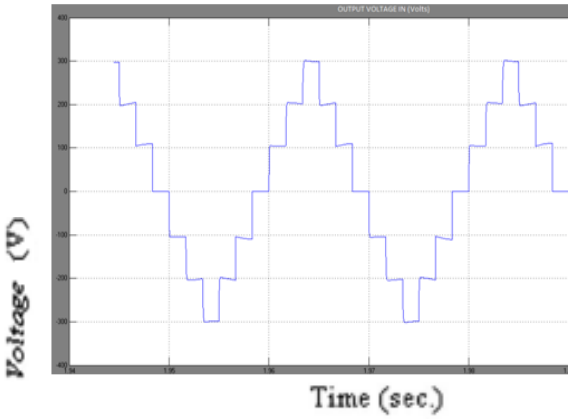

Fig. 5 Experimental output voltage waveform

Experimental output current waveform for impedance source seven level cascaded multilevel inverter is shown in Fig. 6. Load used for this simulation is resistive load of 50Ω. So the output current will be 6A. This can be observed in below output current waveform.

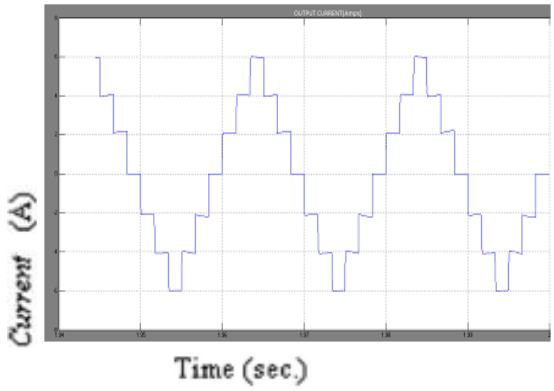

Fig. 6 Experimental output current waveform

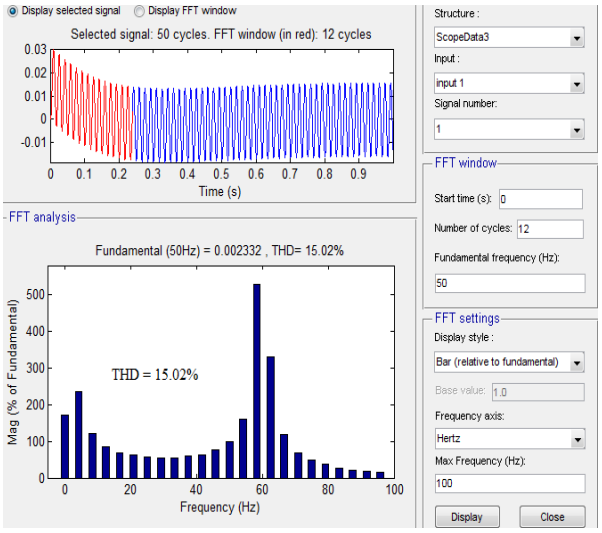

Fig. 7 Measured THD

For the above experimental output waveform THD of 15.02% is obtained which is shown in above Fig. 7.

VII.CONCLUSION

From the simulation output of impedance source cascaded multilevel inverter the ripple contents and the harmonics in the output voltage of the inverter is reduced. Impedance source cascaded multilevel inverter topology have ability to produce any desired output ac voltage, even greater than the line voltage, regardless of the input voltage, thus reducing motor ratings and provide ride-through during voltage sags without any additional energy storage elements and impedance network in each bridge can do both buck and boost operation based on the values of inductors and capacitors in the network. The presented simulation results have been obtained by using MATLAB sim power system tool.

VII.REFERENCES

[1] S. Rajakaruna and Y.R.L. Jayawickarma, "Designing Impedance Network of Z-Source Inverters," in Proceedings IPEC'05, Volume2, pages 962-967, 2005.

[2] Fang Zheng Peng, "Z-Source Inverter for Motor Drives," in *Proceedings IEEE Power Electronics Specialists Conference*, pp. 249-254, Germany, 2004.

[3] F. Z. Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504 – 510, Mar./Apr. 2003.

[4] B. K. Bose, *Power Electronics and Variable Frequency Drives*. UpperSaddle River, NJ: Prentice- Hall, 2002.

[5] P.W. Hammond, "Medium voltage pwm drive and method,"U.S. Patent 5 625 545, April 1997.

[6] M. D. Manjrekar, P. K. Steimer, and T. A. Lipo, "Hybrid multilevel power conversion system: a competitive solution for high power applications,"*IEEE Trans. Ind. Applicat.*, vol. 36, pp. 834–841, May/June 2000.

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