Modeling and behavioral simulation of noise transfer characteristics of a 2 GHz phased-locked loop for frequency synthesizer

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ABSTRACT

We present here an analytical phase noise model of phased-locked loop for frequency synthesizer and its simulation in GHz frequency range. The noise model has been derived and simulated considering two different filter sections in the loop of the phased-locked loop model, namely: (i) active lag-lead filter and (ii) standard feedback approach. The noise transfer functions of the phased-locked loop frequency synthesizer are derived in s-domain for analysis. The mathematical model and analysis for the five main noise transfer functions which are existed in the system have been derived for analysis. The simulation of the phase noise is performed by using MATLAB (Version: 7.1). Here we will discuss in details the procedure for mathematical derivation of the noise model for both active leg-lead filter and filter with standard feedback approach in the loop, its simulation and their results.

Key words: phase noise, transfer function, s-domain analysis, and frequency synthesizer.

1. INTRODUCTION.

Phase noise consists of small random perturbations in the phase of the signal, i.e. phase jitter. An ideal signal source would be able to generate a signal in which the phase advanced at a constant rate. This would produce a single spectral line on a perfect spectrum analyzer. Unfortunately all signal sources produce some phase noise or phase jitter, and these perturbations manifest themselves by broadening the bandwidth (BW) of the signal.

The phase noise is the most important performance criterion of the phased-locked loop (PLL) frequency synthesizer for its stringent requirement in many applications. The problem with phase noise is made worsen in high-frequency applications, since the oscillator phase noise at a given frequency offset typically increases in proportion to the carrier frequency. The noise in PLL is classified into two categories, which are: (a) amplitude noise and (b) phase noise. Amplitude noise can be detected and removed easily. In contrast, phase noise is difficult to identify and express in an equation. This is due to unpredictable characteristics of electronic components.

The world wide communication technology grows dramatically and continuously, especially in the field of wireless communication [1]. The mobile phones have become the basic gadgets for most of the people. Due to this growth, it is important to study the characteristic of the phase noise because it affects the system performance. The phase noise of frequency synthesizers is a key figure of merit in RF communications system designs. Higher than desired phase noise can cause degraded system performance in terms of reducing the signal to noise ratio (SNR), increasing adjacent channel power, and reducing adjacent channel rejection. Besides, in transmitters, local oscillator noise is amplified by the subsequent amplifier stages and is eventually fed to the antenna together with the wanted signal. The required signal is therefore surrounded by a band of noise originating from the phase noise of the local oscillator. So, the noise generated can spread over several KHz masking nearby lower power stations.

1.1 Related works

There are numerous examples of PLL noise modeling in literature. Amit Mehrotra computed PLL output spectra with the help of phase noise of VCO, LF and PD in the year 2002 [2]. In the year 2005, Michael H. Perrott studied phase noise performance by entering various noise parameters in PLL design assistant program [3]. S. A. Osmany, F. Herzel, K. Schmalz, and W. Winkler presented an analytical model for fractional -N-PLL with emphasis on integrated RF synthesizer in GHz range in the year 2007 [4]. In the year 2007, Lin Jia, Kiat Seng Yeo Jian Guo Ma, Manh Anh Do, Xiao Peng Yu derived Noise transfer functions (TF) of PLL based synthesizers and studied stability of the system [5]. Ashok Swaminathan, Kevin J. Wang, and Ian Galton presented a fast-settling adaptive calibration technique that makes phase noise canceling $\Delta\Sigma$ fractional-N PLLs for the low reference frequencies commonly used in wireless Communication systems in 2007. The technique is demonstrated as an enabling component of a 2.4 GHz ISM band CMOS PLL IC with a BW of 730 KHz, a 12MHz reference, and an on-chip loop filter [6].

Keeping in view of the above, to improve the performance of the receiving and transmitting terminal of wireless communication system, we have designed an analytical phase noise model of PLL and simulate it in GHz frequency range to study the phase noise of PLL. The details of our present study are presented in this paper.

2. MATHEMATICAL MODEL OF PHASE NOISE

The PLL is a feedback control system used to lock the output frequency and phase to the frequency and phase of an input signal. It can also be used as a frequency synthesizer for modulation and demodulation. Normally, PLL is used in both transmitting and receiving terminals for any wireless communication systems. It composed of several units, namely (i) phase frequency detector (PFD), (ii) low pass loop filter (LPF), (iii) voltage controlled oscillator (VCO) and (iv) frequency divider (FD). The function of the PD is to generate an output waveform based on the difference in phase (and frequency) between the input signals. The low-noise reference signal which is low-pass filtered is applied to the controlling node of the VCO. If the input signal frequency is within the VCO tuning range, the VCO output is also "locked" to the same frequency, because the input signal and the phase difference between the two signals is very small. The frequency divider in the feedback path is usually used to generate a low noise, high frequency signal from a low frequency low noise oscillator. The frequency division may be performed using an analog divider or by a digital synchronous and asynchronous counter. [7]

The block diagram of the main noise sources in a PLL are modeled in fig. 1, which includes (a) reference noise, (b) VCO noise, (c) PFD noise, (d) LPF noise and (e) FD noise. This noise model of the PLL is a very important requirement in most of the applications in communications. Every building block of the PLL contributes to the total output noise.
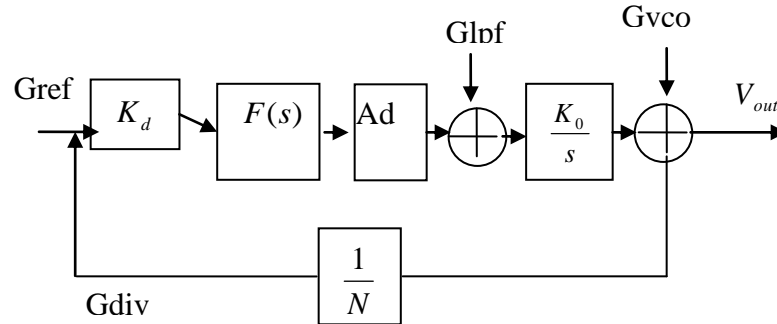

Fig.1: Noise distribution in PLL

2.1 The reference noise

A low noise reference is crucial for a good PLL performance. Although the phase noise of reference is typically lower than that of VCO output noise, it may become comparable to the VCO noise. The TF from the reference source to the PLL output is given by [4, 5, 8],

$$G_{ref} = \frac{Forwardgain}{1+Loopgain} \tag{1}$$

The loop gain G of the system model is the product of individual transfer function (TF) of the different blocks used in the system design. So, the loop gain G for the present PLL model can be expressed as [9]:

$$G = \frac{A_d K_d F(s)(\frac{K_0}{s})}{N}$$
$$= \frac{A_d K_d F(s) K_0}{Ns} \tag{2}$$

In equation (2)

K_d = Phase detector gain factor (volts/radian)

K_0/s = VCO gain factor (Hz/volt)

N = Division ratio

A_d = Amplifier gain

$F(s)$ = Loop filter TF

Accordingly, the forward gain of the model can be expressed as [9]:

$$Forwardgain = K_d F(s) \frac{K_0}{s} A_d \tag{3}$$

Therefore,

$$G_{ref} = \frac{K_d F(s) \dfrac{K_0}{s} A_d}{1 + \dfrac{A_d k_d F(s) K_0}{Ns}} \tag{4}$$

Now, putting the TF of the active lag-lead filter (ALLF) for F(s) in equation (4) results [10],

$$G_{ref} = \frac{K_d (\dfrac{1 + sCR_2}{sR_1C}) \dfrac{K_0}{s} A_d}{1 + A_d K_d (\dfrac{1 + sCR_2}{sR_1C}) \dfrac{K_0}{Ns}}$$

$$= \frac{sCR_2 + \dfrac{A_d K_d K_0}{N}}{s^2 R_1 C + \dfrac{A_d K_d K_0}{N}(1 + sCR_2)} \tag{5}$$

Similarly, putting the TF of the LF section in the loop using standard feedback approach (SFA) in equation (4) results [10],

$$G_{ref} = \frac{K_d (\dfrac{1 + sR_2C_2}{s^2 C_1 C_2 R_2 + s(C_1 + C_2)}) \dfrac{K_0}{s} A_d}{1 + A_d K_d (\dfrac{1 + sC_2 R_2}{s^2 R_2 C_1 C_2 + s(C_1 + C_2)}) \dfrac{K_0}{Ns}}$$

$$= \frac{K_d K_0 A_d (1 + sR_2 C_2)}{s^3 C_1 C_2 R_2 + s^2 (C_1 + C_2) + (1 + sR_2 C_2) \dfrac{A_d k_d K_0}{N}} \tag{6}$$

2.2 The VCO Noise

The oscillators are responsible for most of the noise at the output of the majority of well designed PLL frequency synthesizers. This is because the oscillators inherently tend to amplify noise generated near their oscillation frequency and any of its harmonics. The VCO noise is high-pass filtered in PLL circuits. The PLL can be used to clean up the VCO phase noise within the loop BW. The VCO phase noise is unattenuated at offset frequencies beyond the BW. At high frequencies, the noise of the PLL is that of the VCO noise. The TF of the VCO's phase noise in s-domain is given as [5, 4, 8]:

$$G_{vco} = \frac{1}{1 + Loopgain}$$

$$G_{vco} = \frac{1}{1 + \dfrac{A_d k_d F(s) K_0}{Ns}} \tag{7}$$

Putting the TF of the ALLF for F(s) in equation (7) results [10],

$$G_{vco} = \frac{1}{1 + \dfrac{A_d k_d (\dfrac{1 + scR_2}{sR_1 c}) K_0}{Ns}} \tag{8}$$

Similarly, putting the TF of the LF section in the loop using SFA for $F(s)$ in equation (7) results [10],

$$H(s) = \frac{1}{1 + A_d K_d (\dfrac{1 + sC_2 R_2}{s^2 R_2 C_1 C_2 + s(C_1 + C_2)}) \dfrac{K_0}{Ns}} \tag{9}$$

2.3 The PFD Noise

The TF for the PD can be obtained as [8, 10]:

$$G_{pdf} = \frac{F(s) \dfrac{K_0}{s}}{1 + \dfrac{A_d k_d F(s) K_0}{Ns}} \tag{10}$$

Putting the TF of the ALLF for F(s) in equation (10) results [10],

$$G_{pdf} = \frac{(\dfrac{1 + scR_2}{scR_1}) \dfrac{K_0}{s}}{1 + \dfrac{A_d k_d (\dfrac{1 + scR_2}{scR_1}) K_0}{Ns}} \tag{11}$$

Similarly, putting the TF of the LF section in the loop using SFA in equation (10) results [10],

$$H(s) = \frac{(\dfrac{1 + sC_2 R_2}{s^2 R_2 C_1 C_2 + s(C_1 + C_2)}) \dfrac{K_0}{s}}{1 + A_d K_d (\dfrac{1 + sC_2 R_2}{s^2 R_2 C_1 C_2 + s(C_1 + C_2)}) \dfrac{K_0}{Ns}} \tag{12}$$

2.4 The LF Noise

The Noise TF for the LF has band-pass characteristics. In the region around the BW of the PLL, the filter noise may sufficiently contribute to the overall phase noise due to the small filter capacitances. The TF is represented as [5, 8]:

$$G_{lpf} = \frac{\dfrac{K_0}{s}}{1 + Loopgain}$$

$$G_{lpf} = \frac{\dfrac{K_0}{s}}{1 + \dfrac{A_d k_d F(s) K_0}{Ns}}$$

(13)

Putting the TF of the LF section in the loop using ALLF in equation (13) results [10],

$$G_{lpf} = \frac{\dfrac{K_0}{s}}{1 + \dfrac{A_d k_d \left(\dfrac{1 + scR_2}{scR_1}\right) K_0}{Ns}}$$

(14)

Similarly, putting the TF of the LF section in the loop using SFA in equation (13) results [10],

$$G_{lpf} = \frac{\dfrac{K_0}{s}}{1 + A_d K_d \left(\dfrac{1 + sC_2 R_2}{s^2 R_2 C_1 C_2 + s(C_1 + C_2)}\right) \dfrac{K_0}{Ns}}$$

(15)

2.5 The FD Noise

The FDs are always followed by some form of edge-sensitive threshold circuit, which implies that the overall noise behavior of the PLL is only influenced by the noise produced by the divider at the time when the threshold is being crossed in the proper direction. The noise produced by the FD is cyclostationary, in a sense that the noise power varies over time. Thus, it is important to analyze the noise behavior of the divider carefully. The TF of FD can be expressed as [8]

$$G_{div} = \frac{2\pi G_{ref}}{Kd}$$

(16)

For ALLF in the loop putting the value of G_{ref} from equation (5) in equation (16) results,

$$G_{div} = \frac{2\pi \left(\dfrac{1 + sCR_2}{sR_1 C}\right) \dfrac{K_0}{s} A_d}{1 + A_d K_d \left(\dfrac{1 + sCR_2}{sR_1 C}\right) \dfrac{K_0}{Ns}}$$

(17)

For SFA in the loop putting the value of G_{ref} from equation (6) in equation (16) results,

$$= \frac{2\pi K_0 A_d (1 + sR_2 C_2)}{s^3 C_1 C_2 R_2 + s^2 (C_1 + C_2) + (1 + sR_2 C_2) \dfrac{A_d k_d K_0}{N}}$$

(18)

3. THE FLOW DIAGRAM AND ALGORITHM OF SIMULATION PROGRAM

The algorithm of the simulation program developed for the present work is given below. The program is developed to evaluate as well for graphical representation of various parameters that influence the noise TF of the proposed model. Simulation programs are developed by considering both ALLF and loop with SFA. The TF **H** is created using the **tf** command for each block of the PLL as shown in fig.1. The **L** and **G** represent the forward loop gain and closed loop gain of the model respectively from which the noise TF of each block of the system is evaluated. Using **bode** function the magnitude of phase noise for different blocks are determined. From those magnitude curves the attenuation value can be easily determined.

The Algorithm

Steps	Instructions	Steps	Instructions
1	enter num, den	16	Gvco=1/ (1+G)
2	H= tf (num, den)	17	bode (G_{vco})
3	evaluate H1	18	evaluate vco phase noise
4	repeat steps 1 & 2	19	Gref=L/ (1+G)
5	evaluate H2	20	bode ($_G$ref)
6	repeat steps 1 & 2	21	evaluate reference input phase noise
7	evaluate H3	22	Gfb= (2*pi*Gref)/k_d
8	repeat steps 1 & 2	23	bode (Gfb)
9	evaluate H4	24	evaluate divider noise
10	repeat steps 1 & 2	25	Glpf=h3/(1+G)
11	evaluate H5	26	bode (Glpf)
12	L=mineral (H1*H2*H3*H4)	27	evaluate loop filter phase noise
13	evaluate forward loop gain L	28	Gpfd= (h2*h3)/ (1+G)
14	G= mineral (L*H5)	29	bode (Gpfd)
15	evaluate loop gain	30	evaluate phase frequency detector noise
		31	end

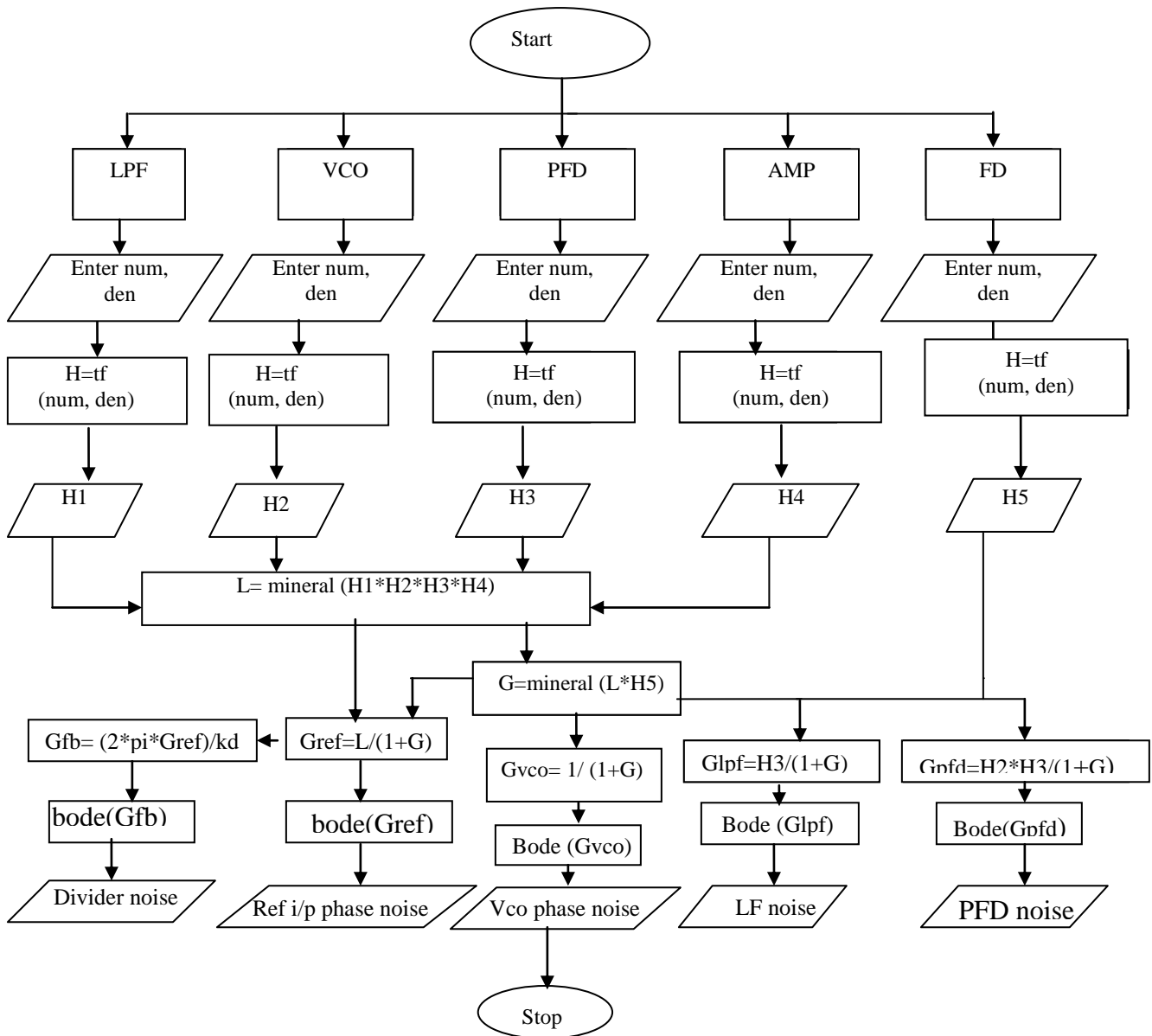The self explanatory flow diagram of the program is shown in fig.2

Fig.2: The Flow diagram

4. THE SIMULATION

Behavioral simulations are carried out to analyze the noise TF of each block's of the PLL. The numerical value of design parameters for the model is given in Table 1 below:

TABLE 1: Numerical value of the design parameters

LOOP	K_D(V/ RAD)	K_0(MHZ/V)	N	R_1	R_2	C_1	C_2	DAMPING FACTOR	PHASE MARGIN
ALLF	0.7	10	50	10 k	10 k	3 pF	-	0.672	78.1^0
SFA	0.7	10	50	100 Ω	-	6 pF	10nF	0.733	56.2^0

The simulations for the noise TF in s domain analysis are carried out using MatLab (Version 7.1). Detailed simulation results are discussed below.

4.1 Simulation for VCO noise TF

Fig.3 (a) shows the simulation response of the present VCO noise model for ALLF and SFA in the loop. The y-axis is the frequency in radian per seconds and x-axis is the noise magnitude in dB. The closed-loop TF of VCO noise behaves as a high pass filter, which allows the high frequency component to transmit, and suppresses the low frequency component [1]. From bode plot analysis of the noise TF, the attenuation can be determined. The simulation response of the present VCO noise model is compared with the earlier work presented elsewhere [5] as shown in fig.3(b). The attenuation for both the cases are almost similar but a peak is observed in the noise magnitude curve of the model with ALLF which may be due to the small damping value ($\zeta < 0.707$). The jitter increases at higher BW due to the additional peaking in the noise TF. The noise peak also causes the system to be unstable [5, 11].
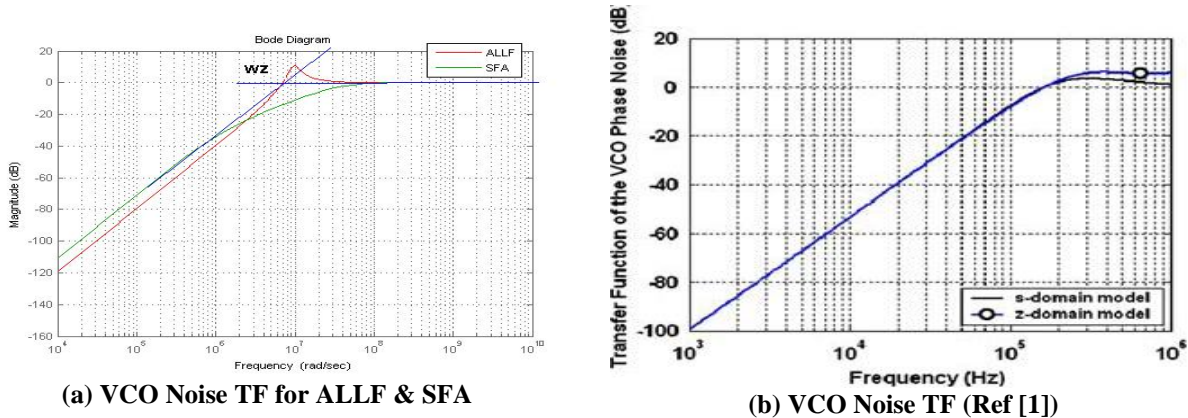

(a) VCO Noise TF for ALLF & SFA   (b) VCO Noise TF (Ref [1])

Fig. 3: Responses for VCO noise TF

4.2 Simulation for LPF noise

Fig.4 (a) shows the simulation response of the present LPF noise model for ALLF and SFA in the loop. The y-axis is the frequency in radian per seconds and x-axis is the noise magnitude in dB. For the LPF, its closed-loop TF behaves as a band pass filter, which has pass band frequencies around the BW as compared with the earlier work presented elsewhere [5] as shown in fig.4(b). In fig.4 (a), an attenuation of -20dB/decade is observed whereas the attenuation of more than -20dB per decade is observed in case of earlier work as shown in fig.4 (b). In comparison to filter section with SFA in the loop, a noise peak is observed in magnitude curve of the model with ALLF, which may be also due to the small damping value ($\zeta < 0.707$).
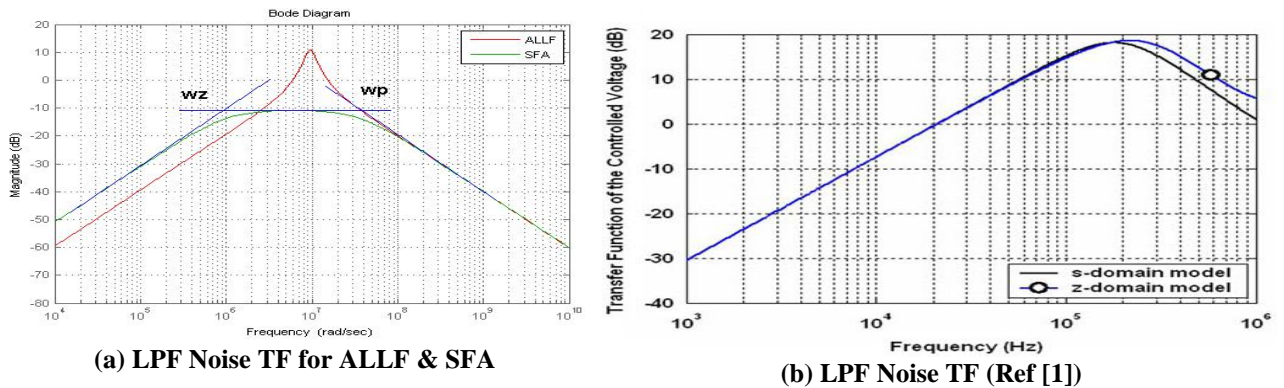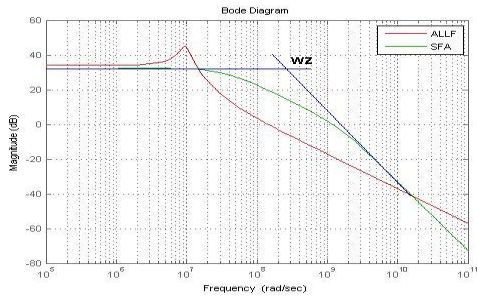

(a) LPF Noise TF for ALLF & SFA   (b) LPF Noise TF (Ref [1])
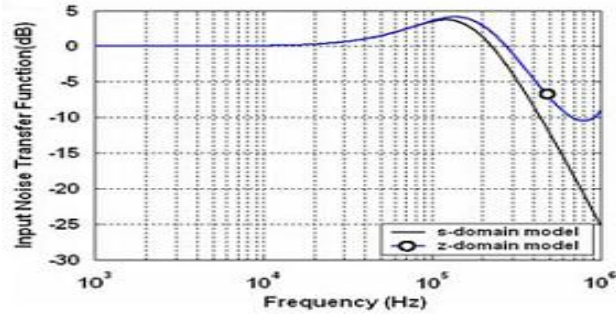
Fig. 4: Responses for LPF noise TF

4.3 Simulation for reference I/P noise

Fig.5 (a) shows the simulation response of the present Ref I/P noise model for ALLF and SFA in the loop. The y-axis is the frequency in radian per seconds and x-axis is the noise magnitude in dB. The closed-loop TF of Ref I/P noise also behaves as a LPF as compared to the earlier work presented elsewhere [5] as shown in fig.5 (b). It is observed that a lower attenuation (-20dB/decade) with a noise peak in the noise magnitude curve of the model is observed with ALLF in comparison to the model with SFA in the loop. This noise peak may be due to small damping value ($\zeta < 0.707$) which may lead to system unstability.
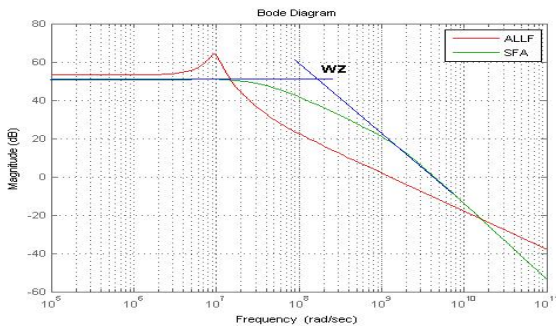

(a) Ref I/P Noise TF for ALLF & SFA

(b) Ref I/P Noise TF (Ref [1])

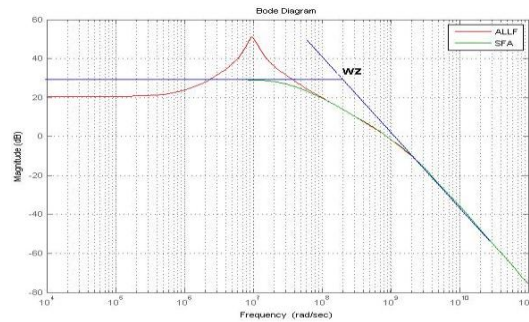**Fig.5: Response for Ref I/P noise TF**

4.4 Simulation for FD and PFD noise

Fig.6 (a) shows the simulation response of the present FD noise model for ALLF and SFA in the loop. The x-axis is the noise magnitude in dB whereas the y-axis represents frequency in radian per seconds. The closed-loop FD noise behaves as a LPF. The FD noise with ALLF shows low attenuation (-20dB/decade) with a noise peak in comparison to the FD noise with SFA in the loop.

The simulation response of the present PFD noise model for ALLF and SFA in the loop are shown in fig. 6(b). Here, x-axis is the noise magnitude in dB whereas the y-axis represents frequency in radian per seconds. The closed-loop PFD noise also behaves as a LPF. The PFD with both ALLF & SFA in the loop show same attenuation value. A noise peak is observed in the magnitude curve of the model with ALLF in the loop, which may be due to the small damping value ($\zeta < 0.707$).
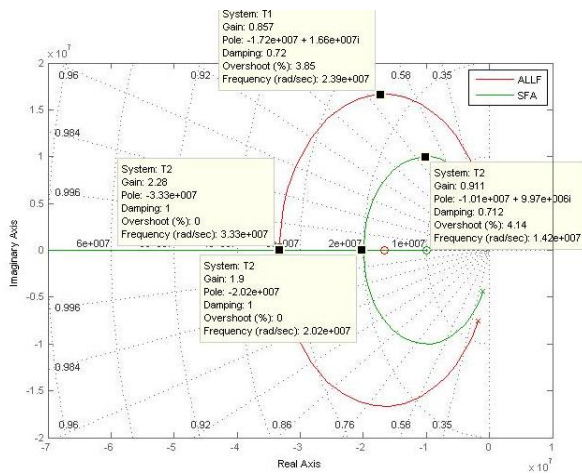

(a) FD Noise TF for ALLF & SFA
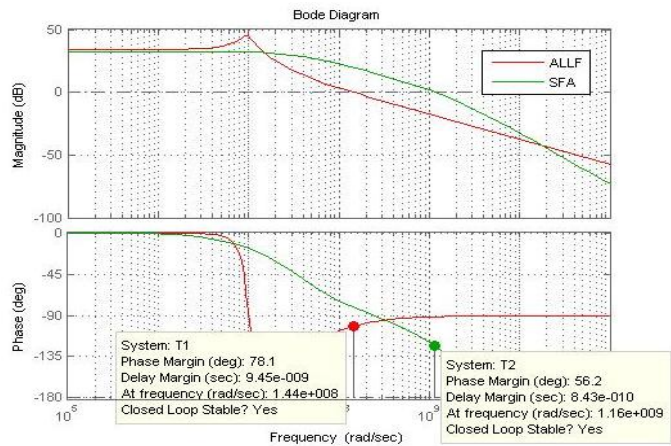
(b) PFD Noise TF for ALLF & SFA

Fig.6: The responses for FD and PFD noises

5. SYSTEM STABILITY

The degree of stability is a crucial feature of any PLL frequency synthesizer. If the system is unstable, it can produce undesirable ringing and longer settling time. Bode plot is a useful tool for evaluating stability. The phase margin of the system is derived from the Bode plot. A PLL frequency synthesizer is stable if the phase margin is positive and unstable if the phase margin is negative [12]. The stability can be also explained in terms of Root Locus analysis. The synthesizer is stable if all poles of the closed loop TF are inside the unit circle in s-plane. Conversely, the system is unstable if any one of the pole is outside the unit circle. The Root locus and Bode plot for the present noise model for ALLF and SFA in the loop is shown in fig.7 and fig.8 respectively.

Fig. 7: The simulated response for Root Locus   Fig. 8: The simulated response for phase margin
(Loop with ALLF & SFA)   (Loop with ALLF & SFA)

The plot of Root Locus in fig.7 shows that all the poles are in the left part of the Root Locus and within the unit circle, which indicates the system stability for both ALLF & SFA. The phase margin plot of fig.8 shows that the phase margin values are 56.2^0 and 78.1^0 respectively. These two values are well within the limit of stability [10].

6. RESULTS AND DISCUSSION

The simulations responses show that the noise VCO, G_{vco} exhibits high pass characteristics. The attenuation decreases at - 40dB/decade below the zero crossover frequency ω_z. At higher frequencies the VCO phase noise is transmitted directly to PLL output with a gain of 0 dB. The noise of LPF, G_{lpf} exhibits band pass characteristics. The attenuation increases at -20dB/decade above zero crossover frequency w_z and decreases at -20dB/decade below the corner frequency ω_p. The reference noise G_{ref}, divider noise G_{div} and the noise of PFD, G_{pfd} exhibits low pass characteristics. The attenuation in each cases decrease at -38dB/decade below the zero crossover frequency ω_z. From the responses of the simulation, it is observed that the responses of each of the three noise exhibited peaks with an ALLF in the loop where as the model with SFA in the loop does not show any peak. The peak always occurs for low pass responses. It is because, for small damping ($\zeta < 0.707$) the complex pole of the TF is near the imaginary axis of the s-plane. The simulation responses for root locus and phase margin indicate that both the noise model with ALLF and SFA in the loops is quite stable. The simulations results are summarizes in Table 2 below:

TABLE 2: Comparison of simulated response parameters with standard and
earlier works

TRANSFER FUNCTION	CHARACTERISTICS	ATTENUATION OBTAINED(DB/ DECADE)	STANDARD ATTENUATION (DB/DECADE)	EARLIER WORK REF [1]
$G_{vco}[s]$	High pass	-40	-40	≈ - 40
$G_{lpf}[s]$	Band pass	-20	-40	≥-20
$G_{div}[s]$	Low pass	-38	-40	N/A
$G_{ref}[s]$	Low pass	-38	-40	-30<attenuation<-40
$G_{pfd}[s]$	Low pass	-38	-40	N/A

6. CONCLUSION

The detailed analysis on modeling and simulations of an analytical phase noise models of PLL frequency synthesizer has been presented here. From our study on the noise model, it is observed that the responses of all the noise TF have existed peaks with an ALLF in the loop where as the model with SFA in the loop does not show any peak. The peak always occurs for low pass responses. It is because, for small damping ($\zeta < 0.707$) the complex pole of the TF is near the imaginary axis of the s-plane. So, initial response effects become prominent [12]. The peaking may also occurs due to the increase in the number of poles and zeros [13]. Also, all the simulated response parameters of the present noise model are well within the predicted standard parameter values and values of earlier work. As such, we can conclude that the model may be suitable for research as well as for industrial applications.

The phase noise model presented in this paper is relatively simple and can be used for accurate phase noise prediction for PLL frequency synthesizer designs. These results will certainly provide PLL developers in research and industrial application to develop their own PLL frequency synthesizer, based on our model, with an indication of the noise performance tradeoffs associated with current technologies.

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