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An Asymmetrical Dc-Dc Converter with a High Voltage Gain

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Abstract: *An asymmetrical full bridge converter is proposed in the paper. The proposed converter achieves zero voltage switching of all the power switches. Zero current switching of all the output diodes are also achieved here. This in turn provides a highly efficienct operation. The proposed converter can provide a high voltage gain and the voltages across the semi- conductor devices are effectively clamped. The converter can be utilised effectively in high voltage applications as embedded systems, renewable energy systems, fuel cells, mobility applications and uninterrupted power supply.*

I. Introduction

The recent growth of battery powered applications and low voltage storage elements are increasing the demand of efficient step-up dc–dc converters. Typical applications are embedded systems, renewable energy systems, fuel cells, mobility applications and uninterrupted power supply. These applications demand high step-up static gain, high efficiency and reduced weight, volume and cost.

Some classical converters with magnetic coupling as flyback or current-fed push-pull converter can easily achieve high step-up voltage gain. However, the power transformer volume is a problem for the development of a compact converter. The energy of the transformer leakage inductance can produce high voltage stress, increases the switching losses and the electromagnetic interference (EMI) problems, reducing the converter be used to reduce the switching losses and the EMI generation. However the voltage stress is higher than in the hard-switching structures and the cost and circuit complexity are increased. Thus, the weight, volume and losses of the power transformer are limiting factors for the isolated dc–dc converters used in embedded applications.

Non-isolated dc–dc converters as the classical boost, can provide high step-up voltage gain, but with the penalty of high voltage and current stress, high duty-cycle operation and limited dynamic response. The diode reverse recovery current can reduce the efficiency when operating with high current and voltage levels. There are some non-isolated dc–dc converters operating with high static gain, as the quadratic boost converter, but additional inductors and filter capacitors must be used and the switch voltage is high.

In order to overcome these problems, an asymmetrical full bridge converter with high-voltage gain is proposed. The limitation of the maximum duty cycle disappears in the proposed topology. The proposed converter features high-voltage gain, fixed switching frequency, soft-switching operations of all power switches and output diodes, and clamped voltages across power switches and output diodes. The reverse recovery problem of the output diodes is significantly alleviated due to an additional inductor at the secondary side. Therefore, the proposed converter shows high efficiency and it is suitable for high-voltage applications.

II. Literature Review

The conventional boost converters are widely employed in power factor correction (PFC) applications due to the simple circuit structure. The conventional single-phase single-switch boost converter is shown in Figure 2.1. In theory, the voltage gain of the boost converter can be infinite when the duty cycle is close to one. However, the switch turn-off period becomes short when the duty cycle increases. The current ripples of the power devices are large, with high-step-up conversion [5], which increases the power device conduction losses and turn-off current. Moreover, the voltage stresses of the switch and the diode are equal to the output voltage, which is large in high output- voltage applications. The cost of the switches with high voltage stress is rather higher than that of the switches with low voltage stress. The switching and reverse-recovery losses are significant due to the hard-switching operation. Furthermore, the power level is limited by the single-phase single-switch solution.

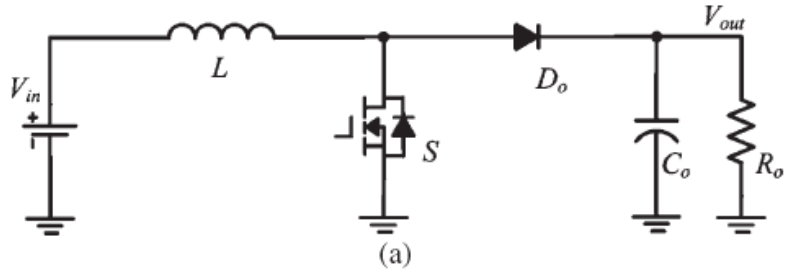


Figure 2.1: Conventional boost converter

The interleaved structure is another effective solution to increase the power level, which can minimize the current ripple, can reduce the passive component size, can improve the transient response, and can realize the thermal distribution. Figure 2.2 shows a two-phase conventional interleaved boost converter. However, the power devices still operate at hard switching [10]. The efficiency is limited because the output diode reverse-recovery problem is still serious in high-output voltage applications.

An active zero current transition (ZCT) interleaved boost converter is derived from the conventional interleaved boost converter by adding a set of auxiliary commutation circuit to each phase [13], which is formed by an active switch, a capacitor, and an inductor. The interleaved boost converter with auxiliary commutation circuits is introduced in Figure 2.3. Turning on of the main switches occurs naturally at zero current, and the output-diode reverse-recovery problem is alleviated due to the critical discontinued current mode (DCM) operation. The auxiliary commutation circuits provide ZCT when the main switch turns off. However, a variable frequency control is mandatory for this converter, which is difficult for the electromagnetic interference (EMI) filter design.

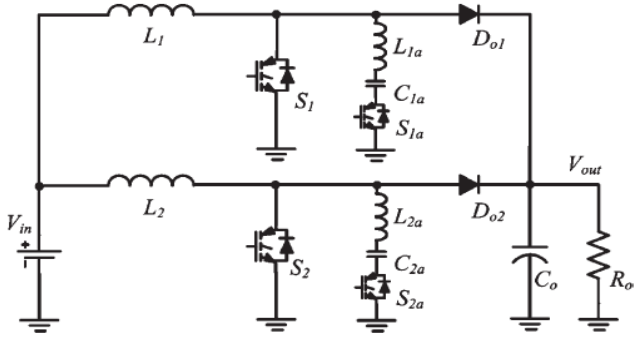


Figure 2.2: Active ZCT interleaved boost converter

The filter inductors of the conventional interleaved boost converter can be integrated into one coupled inductor to reduce the magnetic components. The output-diode reverse recovery problem can be alleviated, and zero current switching (ZCS) turn-on of the switches can be achieved due to the leakage inductance of the coupled inductor.

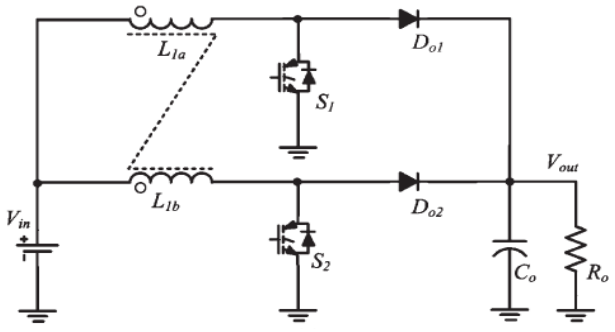


Figure 2.3: Interleaved boost converters with coupled inductor

An active zero-voltage ZCS (ZVZCS) interleaved boost converter with a coupled inductor I shown in Figure 2.5. An auxiliary circuit, which is composed of only a clamp switch and a small capacitor, is inserted into each phase of the interleaved boost converter with coupled inductor. ZCS turn-on and ZVS turn-off are achieved for the main switches. The ZVS soft-switching performance is realized for the auxiliary switches during the

whole switching transition. The leakage inductance of the coupled inductor is used to control the output diode turn-off current falling rate, which alleviates the diode reverse-recovery problem. The converter is symmetrical and suitable for high-power and high-efficiency dc/dc applications.

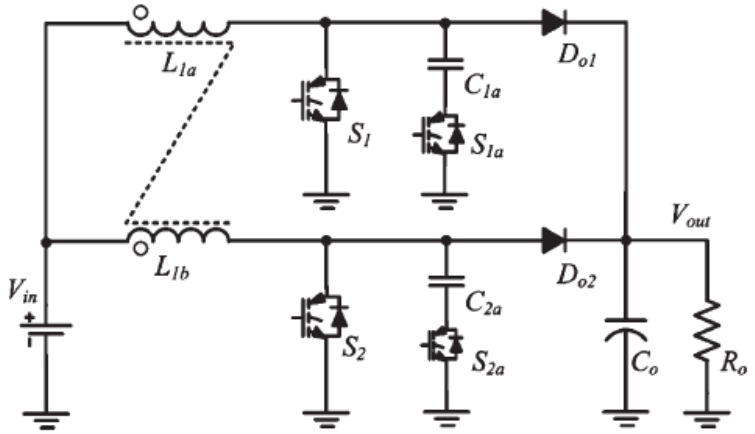


Figure 2.4: Active ZVZCS interleaved boost converter with a coupled inductor

A lot of other active or passive lossless soft-switching solutions are proposed to reduce the switching and reverse-recovery losses that exist in the conventional boost converters. However, most of the improvements are presented for PFC applications. They are not suitable for high-step-up and high efficiency PV grid-connected applications.

The current-fed converters are often used in high step-up applications due to their inherent low input current ripple characteristic and high-voltage gain [11], [12]. However, in the current fed converters, the voltage stresses of the switches are serious. In order to clamp the voltages across the switches and provide zero-voltage switching (ZVS) features, active snubbers are often employed. The snubbers require additional switches and cause additional conduction losses. As a result, the system efficiency decreases. On the other hand, the voltage-fed converters such as phase-shift full-bridge (PSFB) converters, which are widely used, show low-voltage stress of the switching devices. PSFB converters feature fixed switching frequency and ZVS of power switches. However, they have some drawbacks including large conduction loss due to circulating current, duty cycle loss, and the voltage spikes across output rectifiers. The large voltage spikes of the output rectifiers are serious problems especially in high-voltage applications. To remedy these problems, many topologies have been proposed in [13]–[18]. In some of them, auxiliary snubber circuits are employed to suppress the voltage spikes at the secondary side. However, the complexity and the overall cost are increased while the system efficiency decreases due to the additional circuits.

The voltage gain can be extended, and the current ripple can be further reduced to satisfy the high-step-up requirements by employing the cascade structure. Figure 2.6 shows a cascade boost converter. The voltage stress of the first stage is low, and it can be operated with a high switching frequency to improve the power density. The second stage can be worked with a low switching frequency to reduce the switching losses. However, the cascade converter requires two sets of power devices, magnetic cores, and control circuits, which is complex and expensive. The system stability of the cascade structure is another big issue, and the control circuit should be designed carefully. The output-diode reverse-recovery problem of the second stage is severe because a high voltage level should be sustained in the high-output-voltage applications.

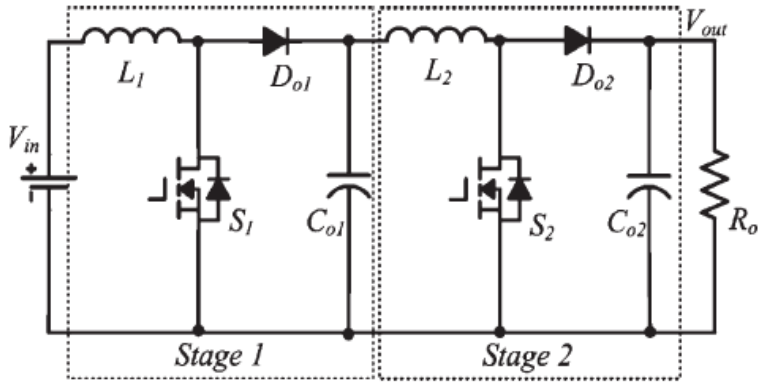


Figure 2.5: Cascade boost converter

The two switches in the cascade boost converter can be integrated into one switch to reduce circuit complexity. The integrated cascade boost converter is shown in Figure 2.7. The inductors *L*1 and *L*2 operate in the charging mode when switch S turns on. The energy stored in *L*1 is transferred to capacitor *C*1 through diode *D*1, and the energy stored in *L*2 is delivered to the load through diode *Do* when switch S turns off. The circuit is simplified, and the instability caused by the cascade structure is avoided, compared with the cascade boost converter.

An integrated cascade boost converter with ZVS soft switching performance is shown in Figure 2.8. The auxiliary circuit is composed of a small inductor *Ls*, a resonant capacitor *Cc*, and a power MOSFET S*c*, which is used to realize the soft switching for the main and clamp switches. However, the switch voltage stress of the integrated cascade boost converters is equal to the high output voltage, and the current stress is large because the current of the inductors *L*1and *L*2 flows through the switch when it turns on. These two factors increase the conduction losses and reduce the circuit efficiency.

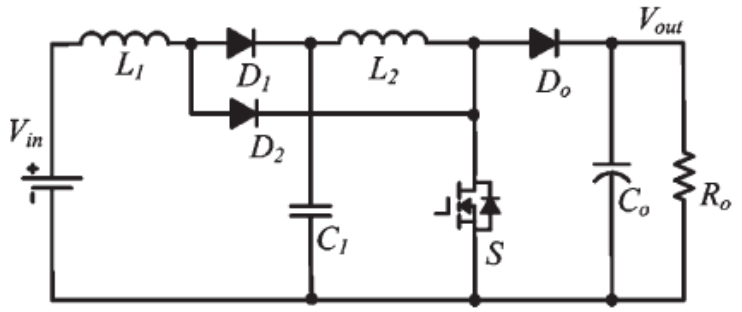


Figure 2.6: Integrated cascade boost converter

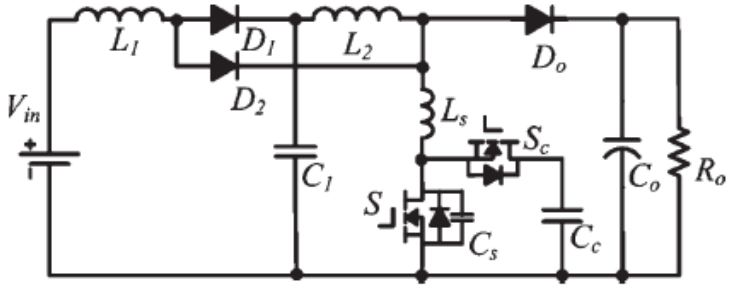


Figure 2.7: Integrated cascade boost converter with ZVS performance

III. Asymmetrical Dc-Dc Converter With High Voltage Gain - Circuit Description

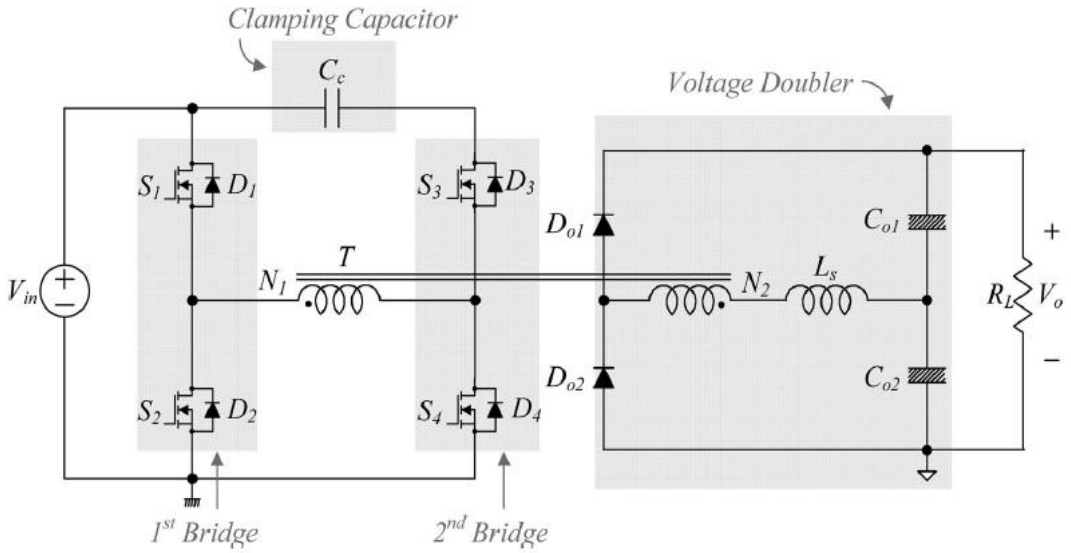


Figure 3.1: Circuit Diagram

The proposed converter has four power switches S1 through S4. There is also the clamping capacitor Cc between top side switches *S*1 and *S*3 of two switch bridges. The voltages across the switches S1 and S2 in the first bridge are confined to the input voltage Vin. The clamping capacitor Cc can clamp the voltages across the switches S3 and S4 in the second bridge. The output stage of the proposed converter has a voltage doubler structure that consists of the secondary winding N2 of the transformer T, the serial inductor Ls, the output capacitors Co1 and Co2 and the output diodes Do1 and Do2. According to the voltage doubler structure, the voltage gain increases and the voltage stresses of the output diodes are confined to the output voltage Vo without any auxiliary circuits.

The equivalent circuit of the proposed converter is shown in Fig. 2. The diodes D1 through D4 are the intrinsic body diodes of all switches. The capacitors C1 through C4 represent their parasitic output capacitances. The transformer *T* is modeled as the magnetizing inductance Lm and the ideal transformer that has a turn ratio of 1:n (n = N2 /N1). Its leakage inductance is included in the serial inductor Ls. To simplify the analysis, it is assumed that the clamping capacitor Cc has a large value and the voltage across Cc is constant as Vc under a steady state. Similarly, the output capacitor voltages are assumed to be constant as Vo1 and Vo2, respectively.

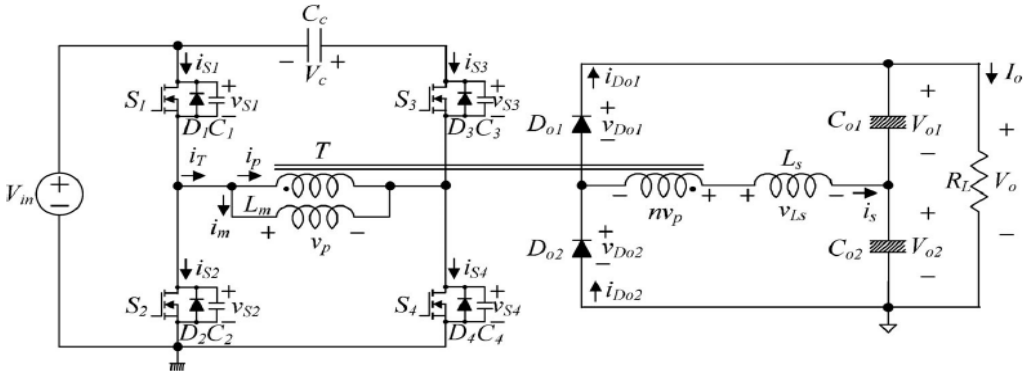
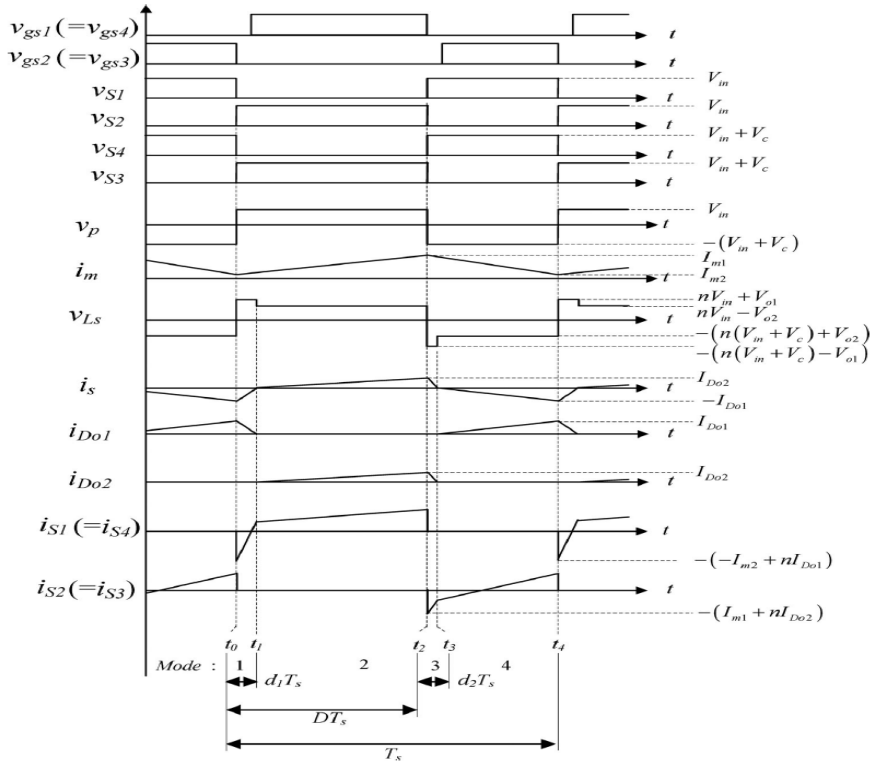


Figure 3.2: Equivalent Circuit

The theoretical waveforms of the proposed converter are shown in Fig. 3. The switch S1 (S4) and the switch S2 (S3) are operated asymmetrically and the duty cycle D is based on the switch S1 (S4). A small delay between driving signals for S1 (S4) and S2 (S3) is a deadtime for the switches. It prevents cross conduction and allows ZVS.



IV. Modal Analysis

The operation of the proposed converter during a switching period T_s is divided into four modes as shown in Fig. 4. Before t_0, the switches S_2 and S_3, and the output diode D_{o1} are conducting. At t_0 , the magnetizing current i_m and the secondary current i_s arrive at their minimum values Im_2 and $-I_{D\,o1}$, respectively.

Mode 1 [t_0, t_1]: At t_0, the switches S_2 and S_3 are turned off. Then, the energy stored in the magnetic components starts to charge/discharge the parasitic capacitances C_1 through C_4. Therefore, the voltages v_{S2} and v_{S3} start to rise from zero. Similarly, the voltage v_{S4} starts to fall from Vin + Vc voltage v_{S1} starts to fall from Vin. Since all the parasitic output capacitances C_1 through C_4 are very small, this transition time interval is very short and it is ignored in Fig. 3. When the voltages v_{S1} and v_{S4} arrive at zero, their body diodes D_1 and D_4 are turned on. Then, the gate signals are applied to the switches S_1 and S_4. Since the currents have already flown through D_1 and D_4 and the voltages v_{S1} and v_{S4} are clamped as zero before the switches S_1 and S_4 are turned on, zero-voltage turn-ON of S_1 and S_4 is achieved. With the turn-ON of S_1 and S_4, the primary voltage v_p across Lm is Vin. Then, the magnetizing current i_m increases linearly from its minimum value Im_2 as follows:

$$i_m(t) = I_{m2} + \frac{Vin}{Lm}(t-t_0)$$

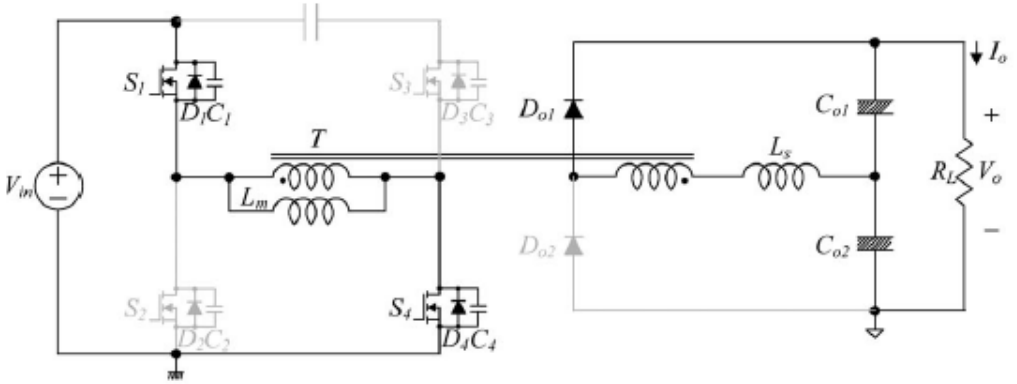


Figure 4.1: Mode 1

Since the voltage V_{Ls} across L_s is $nV_{in}+V_{o1}$, the secondary current is increases from its minimum value $-I_{Do1}$ as follows:

$$i_s(t) = -I_{D01} + \frac{nVin + Vo1}{Ls}(t-t_0)$$

Mode 2 [t_1, t_2]: At t_1, the currents i_s and i_{Do1} arrive at zero and the diode D_{o1} is turned off. Then, the output diode D_{o2} is turned on and its current increases linearly. Since the current changing rate of D_{o1} is controlled by the serial inductor L_s, its reverse-recovery problem is significantly alleviated. Since the voltage $v_{Ls\ is}$ ($nV_{in}-V_{o2}$) in this mode, the current is are given by:

$$i_s(t) = \frac{nVin - V02}{Ls}(t-t_1)$$

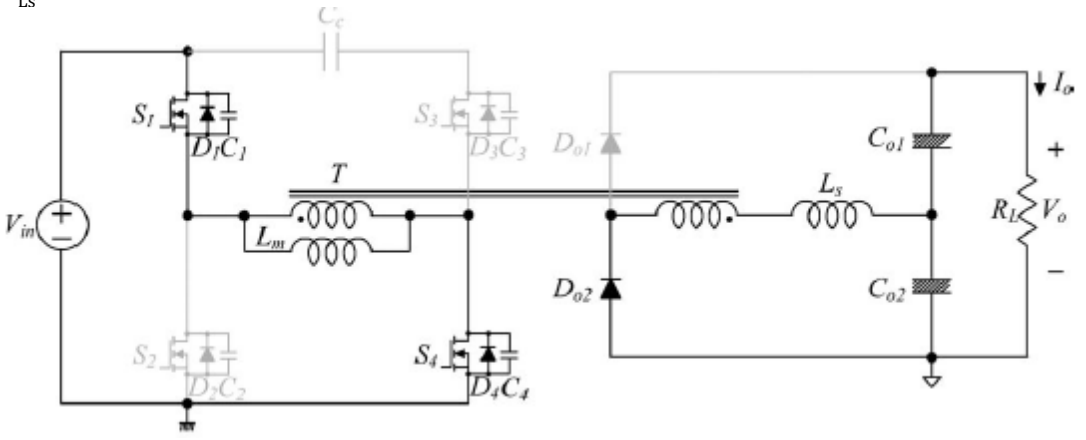


Figure 4.2: Mode 2

At the end of this mode, i_m and i_s arrive at their maximum values I_{m1} and I_{D02}, respectively.

Mode 3 [t_2, t_3]: Similar to mode 1, the switches S_1 and S_4 are turned off at t_2. The parasitic capacitors C_1 and C_4 start to be charged from zero, whereas the parasitic capacitors C_2 and C_3 start to be discharged from V_{in} and V_{in} + V_c, respectively. With the same assumption as mode 1, this transition time interval is very short and it is

ignored in Fig. 3. After the parasitic capacitors are fully charged and discharged, the voltages $v_{S\,2}$ and $v_{S\,3}$ become zero and the body diodes D_2 and D_3 are turned on. Then, the gate signals are applied to the switches S_2 and S_3. Since the currents have already flown through D_2 and D_3 and the voltages $v_{S\,2}$ and $v_{S\,3}$ are clamped as zero, zero-voltage turn-on of S_2 and S_3 is achieved. With the turn-on of S_2 and S_3, the voltage v_p across Lm is $-(V_{in}+V_c)$. Then, the current i_m decreases linearly from its maximum value I_{m1} as follows:

$$i_m(t) = I_{m1} - \frac{Vin + Vc}{Lm}(t\text{-}t_2)$$

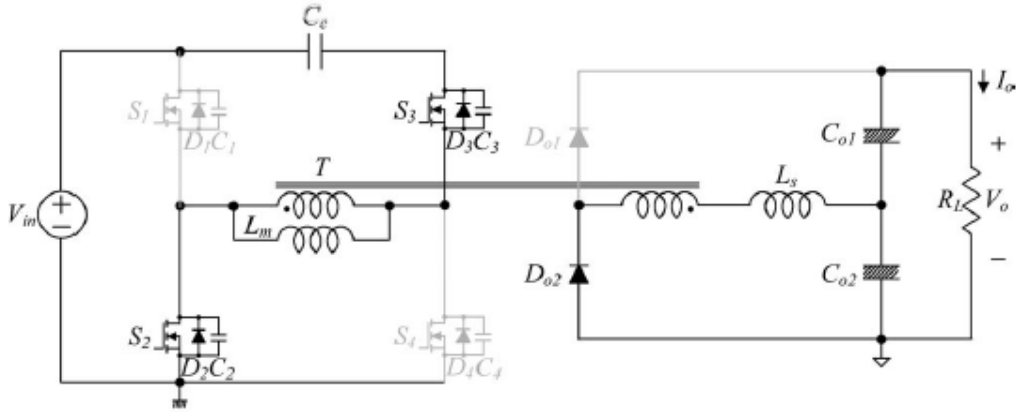


Figure 4.3: Mode 3

Since the voltage v_{Ls} across L_s is $-(n(V_{in} + V_c) + V_{o\,2})$, the current is decreases from its maximum value I_{Do2} as follows:

$$i_s(t) = I_{D02} - \frac{n(Vin + Vc) + V02}{Ls}(t\text{-}t_2)$$

Mode 4 [t_3, t_4]: Similar to mode 2, the currents i_s and i_{Do2} arrive at zero and the diode D_{o2} is turned OFF at t_3. Then, the output diode D_{o1} is turned on and its current increases linearly. Since the current changing rate of D_{o2} is controlled by L_s, its reverse-recovery problem is significantly alleviated. Since the voltage v_{Ls} is $-(n(V_{in} + V_c) - V_{o1})$, the current i_s is given by:

$$i_s(t) = -\frac{n(Vin + Vc) - V01}{Ls}(t\text{-}t_3)$$

At the end of this mode, the currents i_m and i_s arrive at I_{m2} and $-I_{Do1}$, respectively.

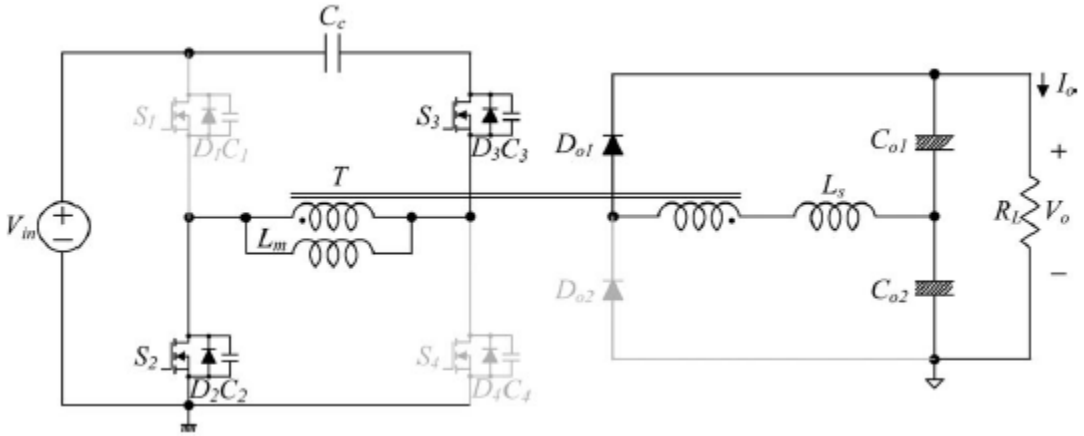


Figure 4.4: Mode 4

IV. Design Parameters

To validate the characteristic of the proposed converter, design procedure is given in this section with the following specifications:

1) Input voltage V_{in} = 48V.
2) Output voltage V_o = 400V.
3) Maximum output power $P_{o,max}$ = 150W.
4) Switching frequency f_s = 74 kHz.

4.1 Selection Dmax and n

The voltage stresses of S3 and S4 depend on D. If they need to be kept below 150V, D should be smaller than 0.75. Therefore, the maximum duty cycle Dmax is determined as 0.7.

Since the required voltage gain is 8.3, the turn ratio n can be calculated as 3 from from the following equation:

$$M = \frac{V0}{Vin} = \frac{n(1-2k)D}{(D+(1-2D)k)(1-D-(1-2D)k)}$$

4.2 Selection of L_s

Serial inductor Ls can be determined as follows:

$$Ls = \frac{nDmaxVinTs}{8Iomax}\,[1-(1-2k)]\text{^}2$$

By using previously selected k∗ and Dmax, (32) gives Ls = 87.5 µH. Then, Ls is selected as 90 µH.

4.3 Selection of L_m

I_{D01} is calculated as 2.287 A from the following equation:

$$Io = \frac{(1-D+d1-d2)IDo\,1}{2} = \frac{(D-d1+d2)IDo\,2}{2}$$

Where, d1 = kD

d2 = k (1-D)

By assuming the output capacitances C_1 to C_4 of the switches as 500pF, we choose Lm<136µH from an inequality which arises since there is current cancellation between i_p and i_m at t_o. Therefore, for ZVS of S_1 and S_4, the energy difference between the energies stored in L_m and L_s should be larger than the energy stored in C_1 through C_4 as follows:

$$-\frac{LmIm\,2\text{^}2}{2} + \frac{LsIDo\,1\text{^}2}{2} > \frac{(C1+C2)Vin\,\text{^}2}{2} = \frac{(C3+C4)(Vin+Vc)\text{^}2}{2}$$

4.4 Selection of C_c

The switch current i_{S3} flows through Cc. From the current waveform i_{S3} in Fig. 3, the resulting ripple in the voltage across Cc depends on the area under the current waveform. The voltage ripple ΔVc across Cc is approximately given by:

$$\Delta Vc = \frac{(1-D)Ts}{4Cc}\,(Im1 + nIDo2)$$

Where,

$$Im1 = Iin + \frac{VinDTs}{2Lm}$$

$$Iin = \frac{VoIo}{Vin}$$

$$IDo2 = \frac{nVin - Vo\,2}{Ls}\,(D\text{-}d1)\,Ts$$

$$Vo2 = \frac{D-d1-(D/(1-D)d2}{D-d1+d2}\,nVin$$

And from the equation for ΔVc, Cc should be larger than 3.49 µF to keep the ripple below 1 V. The value of Cc is selected as 6.6 µF.

4.5 Selection of C_{o1} and C_{o2}

The secondary current i_s flows through C_{01} and C_{02} equally. The voltage ripple across C_{01} is given by:

$$\Delta Vo1 = \frac{(D-d1+d2)TsIDo\,2}{4Co\,1}$$

And from the above equation, C_{01} should be larger than 18.75 µF to keep ΔV_{01} below 0.1 V. The value of C_{01} is selected as 47 µF. Similarly, C_{02} is also selected as 47µF.

V. Simulation Results

The circuit has been simulated using the software, MATLAB/SIMULINK. MATLAB (matrix laboratory) is a numerical computing environment and fourth generation programming language. Developed by Math Works, MATLAB allows matrix manipulations, plotting of functions and data, implementation of algorithms, creation of user interfaces, and interfacing with programs written in other languages, including C, C++, Java and Fortran.

Simulink, developed be Math Works, is a data flow graphical programming language tool for modelling, simulating and analyzing multi- domain dynamic systems. Its primary interface is a graphical block diagramming tool and a customizable set of block libraries. It offers tight integration with the rest of the MATLAB environment and can either drive MATLAB or be scripted from it.

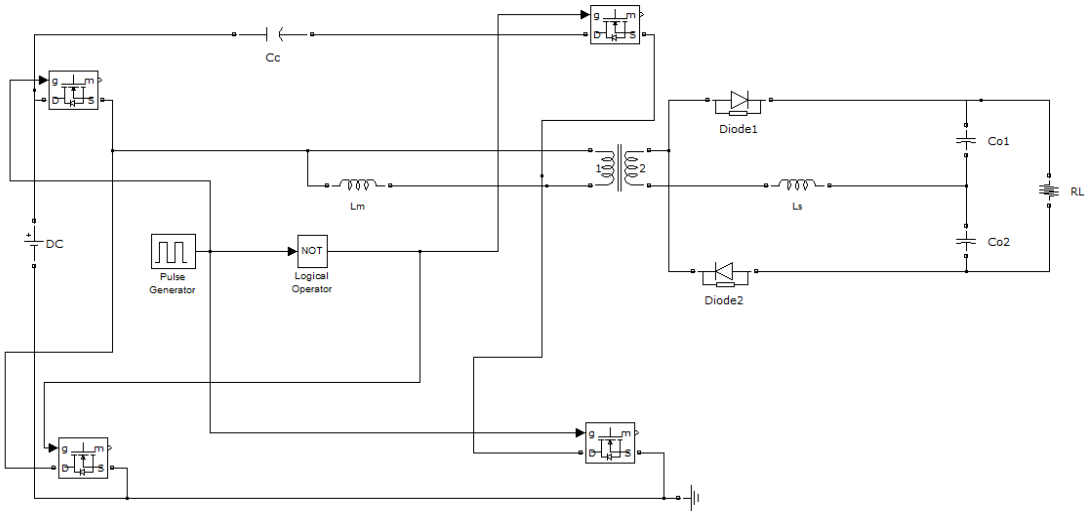


Figure 6.1: MATLAB/SIMULINK model of the circuit

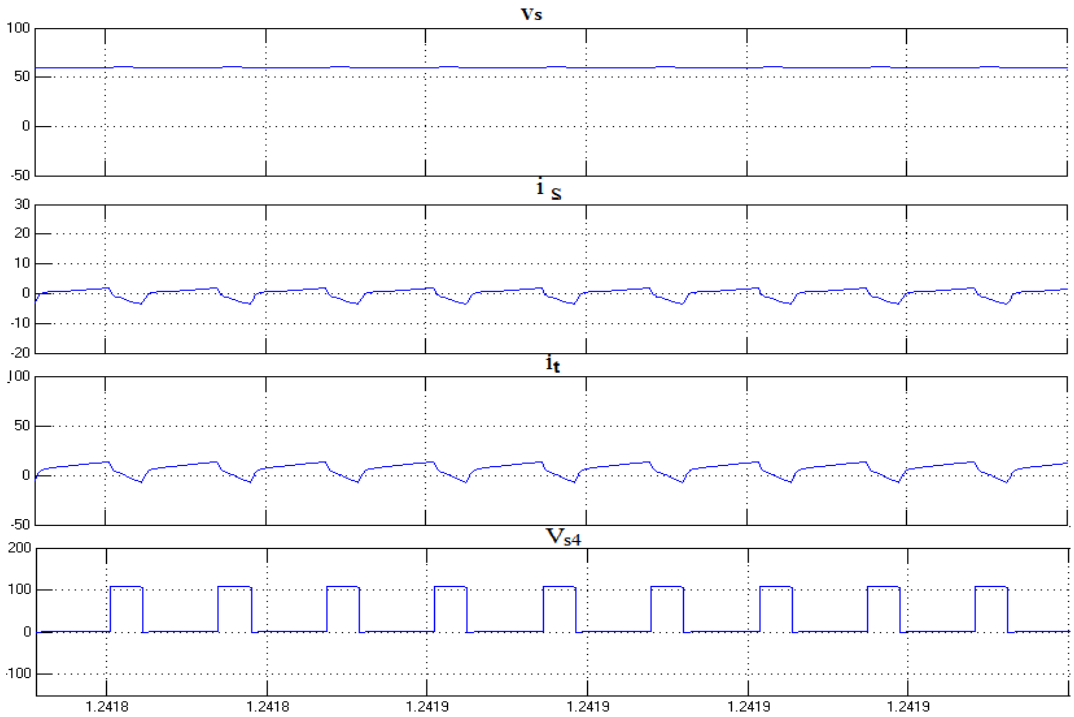


Figure 6.2: Measured Key Waveforms

The figure shows the key waveforms of the proposed converter. It shows the currents is and it, the clamping capacitor voltage Vc and the switch voltage vs2. According to the equation for Cc, clamping capacitor voltage Vc should be 64 v. It agrees with the experimental result. The measured maximum voltage stress of S4 is around 110v, which agrees with the theoretical analysis.

The ZVS operations of all power switch S4 is shown in the figure 6.3. The voltage across the switches goes to zero before the gate pulses are applied to the switches. Since the switch voltages are clamped to zero before the gate pulses are applied, the ZVS turn on of the switches is achieved. Figure 6.4 shows the ZCS of output diodes. After the diode currents fall to zero, the voltages across the diode rise to output voltageV_0. Therefore, the ZCS turn off of the output diodes is achieved.

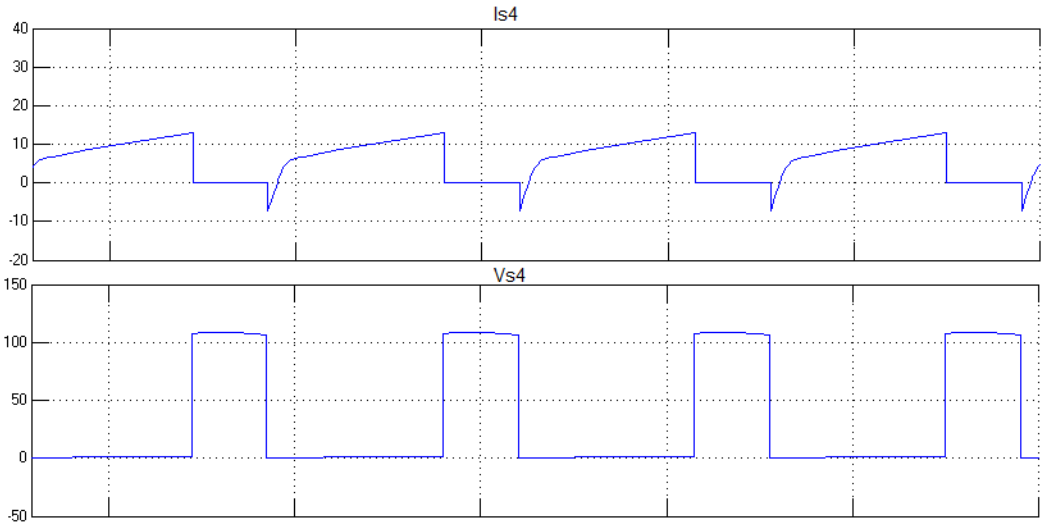


Figure 6.3 ZVS of Switch S4

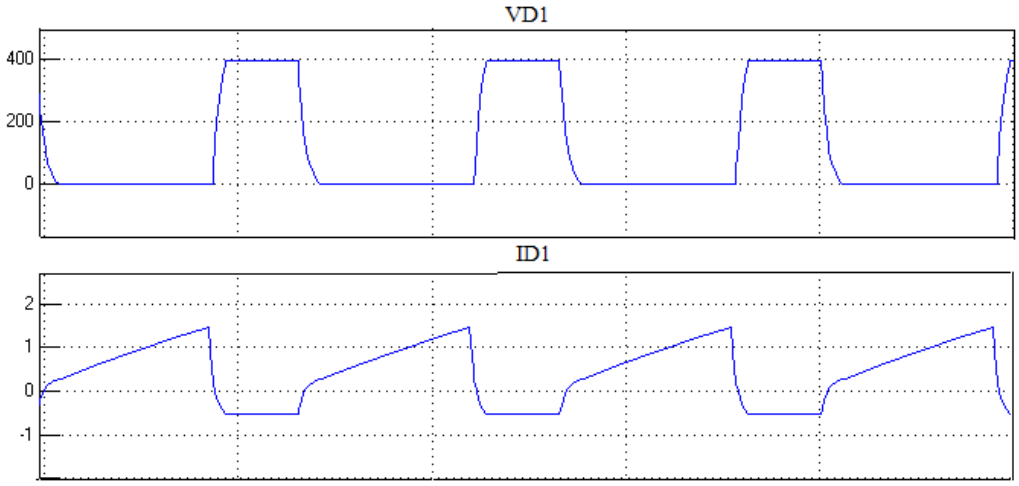


Figure 6.4: ZCS of Diode D1

VI. Conclusion

The limitations of the conventional dc-dc converters in high-step-up, low-cost, and high-efficiency are analyzed. From the aforementioned analysis, the major challenges in applications requiring high voltage gain can be drawn as follows:

1) Extension of voltage gain.
2) Reduction of switch
3) Realization of soft-switching performance to reduce the switching losses.
4) Alleviation of the output-diode reverse-recovery problem to reduce the reverse-recovery losses.

In this paper, an asymmetrical full-bridge converter with high voltage gain has been presented. The ZVS of all power switches and ZCS of the output diodes are achieved. The proposed converter is able to provide a high efficiency and high-voltage gain with relatively low transformer turn ratio. Also, without any auxiliary circuits, the voltages across the switches and the output diodes are effectively clamped. Therefore, the proposed converter is suitable for high-voltage applications. A prototype was simulated to verify the performance of the proposed converter. The voltage gain is 8.3with the transformer turn ratio of 3.

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