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Design of 8-Bit Comparator Using 45nm CMOS Technology

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Abstract: In this paper design of 8- bit binary comparator using 45nm CMOS technology is discussed. This design needs less area and less number of transistors, also discussed about power and execution time. The circuit has three output X, Y and Z. X is active high, when A>B, Y is active high when A=B and Z is active high when both X and Y are active low. Design 1- bit comparator with the help of precharge gate.The design of 1-bit comparator has been extended to implement an 8-bit comparator by connecting in series with pass transistor between them. The design has been implemented in Microwind3.1, is tested successfully and has been validated using Pspice for different measurable parameter.

Keywords: *Power, VLSI, 45nm CMOS technology, area, no of transistors, execution time.*

I. Introduction

Binary comparator is widely used in digital system to compare between two numbers. Binary comparators are found in a wide variety of circuits, such as microprocessors, communications systems, encryption devices, and many others. A faster, more power efficient, or more compact comparator would be an advantage in any of these circuits. A circuit that compares two binary numbers is called comparator. It also decides whether both numbers are equal or not equal.

In this paper, we present two CMOS unsigned binary comparators. Our approaches is first to design 1-bit comparator as one component and then generate its symbol to design 8-bit comparator.

Here we use Microwind3.1 to draw the layout of the CMOS circuit. Then we extract the spice file in Microwind3.1 and run under PSPICE to get the simulation.

II. Previous Work

The current mode signal processing using CMOS technology has gained great interesting circuit designing. With the shrinkage of feature size and increasing demand of high speed and low power application, the current-mode circuit has been considered to be an alternative to voltage-mode circuit. Current comparator is fundamental component of analog system because of better accuracy, low noise and low power consumption. It can be used in A/D converters, oscillators, current to frequency converters, VLSI neural network, sensor circuit and portable wireless communication etc. H. Traff [1] proposed the first high speed, low input impedance current comparator using a simple inverter. Tarff's approach has been modified by a number of designs, A. T. K. Tang et al. [2] and L. Ravezzi et al.[3], where speed increases have been attained at the cost of an increase in power consumption.

Several previous high-speed comparator designs have been proposed. In all[6]precharged function block is attached to several feedback transistors which add extra discharge paths, thus reducing the comparator's delay. However, the precharge period is not utilized for any computation, so the design is not as fast as our high-speed design, as we will show in the sequel.

It is desirable that comparators must provide high speed and low power consumption. Here we need to design such kind of a comparator which compares the value of two 8-bit numbers and output X becomes to 1 when the first number A is larger than the second number B, output Y becomes to 1 when the two numbers A and B are equal and Z becomes 1 when both X and Y becomes zeros.

III. 1-Bit Comparator

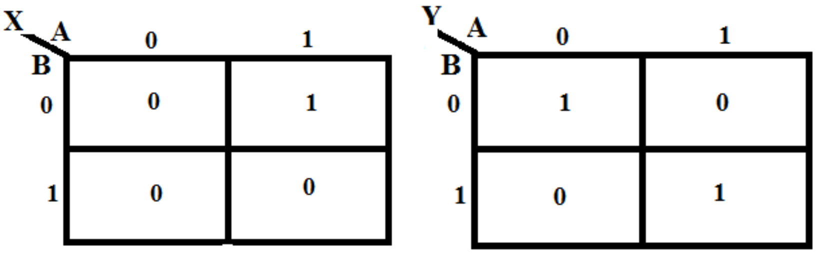
First of all we need to design a 1 bit comparator. We can easily make such a component, 2 bits for input A and B, and 2 bits for output X and Y. X is one when A is larger than B which means only when A is one and B is zero will set X to one. And for the Y, only when A and B both become one and zero will it be set. Here we can define.

X as X=A.B'

Y as Y = A.B +A'.B

Z as Z= (A+B)'

Second we draw the Karnaugh-map of 1-bit comparator and find the relationship between the input and the output.



X =A.B' (When A>B) Y =A.B +A'.B' (When A=B)

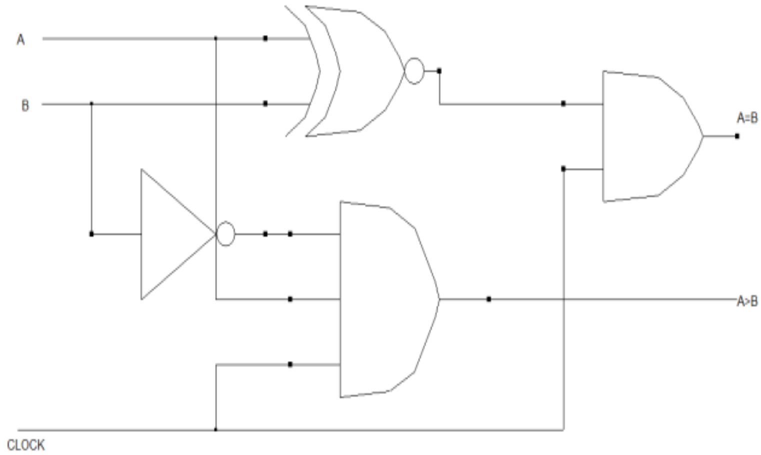


Fig.3.1. Schematic of conventional 1-bit comparator

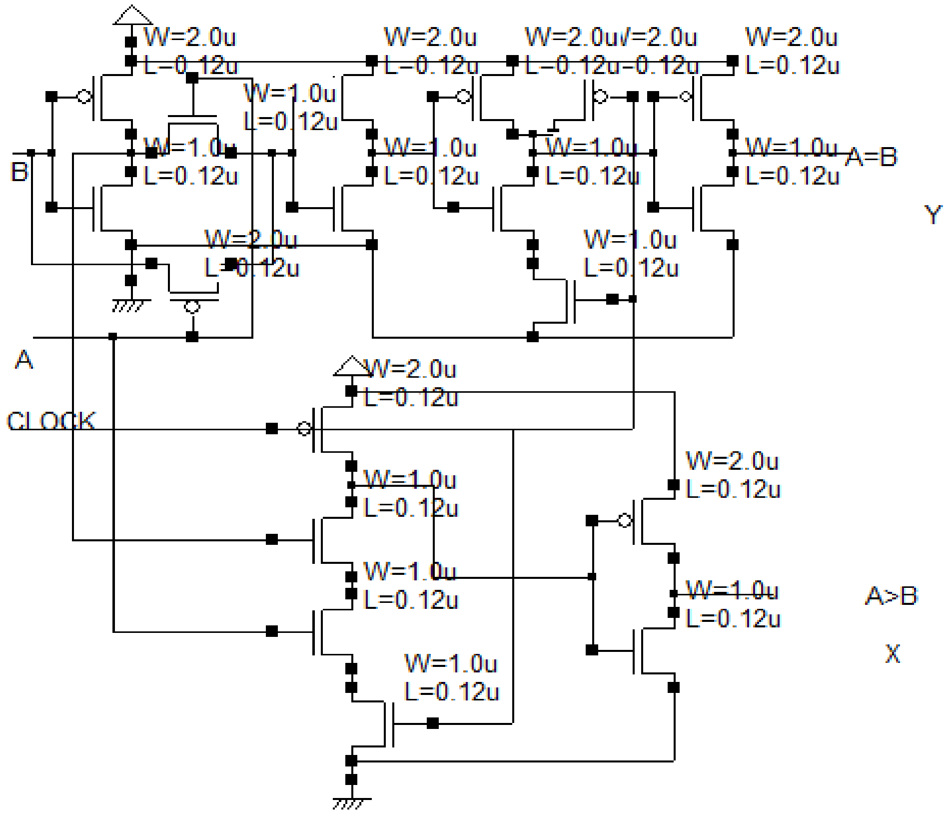


Fig.3.2. Schematic of 1-bit comparator (proposed)

The layout of one bit comparator in Microwind3.1 isshown in fig.3.3

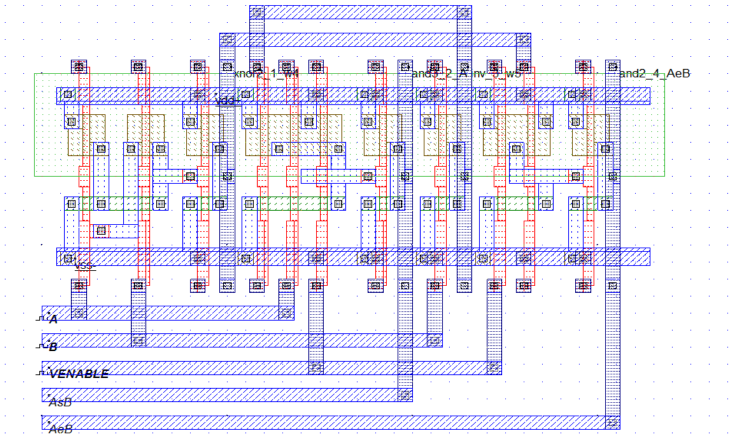


Fig.3.3. Layout of 1-bit conventional comparator

IV. 4-Bit Comparator

The implementation of 4- bit comparator is easy, byconnecting four 1-bit comparator in series. It consist off four one bit comparator, one four input OR gate and one NOR gate. It has three outputs X, Y and Z. Output X becomes high when input A is greater than B (Where A and B is the input), output Y becomes highwhen both inputs are equal. When both X and Y output are low then in thatcase output Z becomes high.

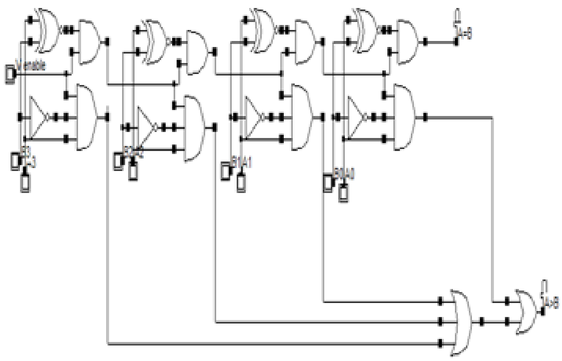


Fig.4.1.Schematic of 4-bit conventional comparator

The layout of Four- bit comparator in Microwind3.1 isshown in fig.4.2.

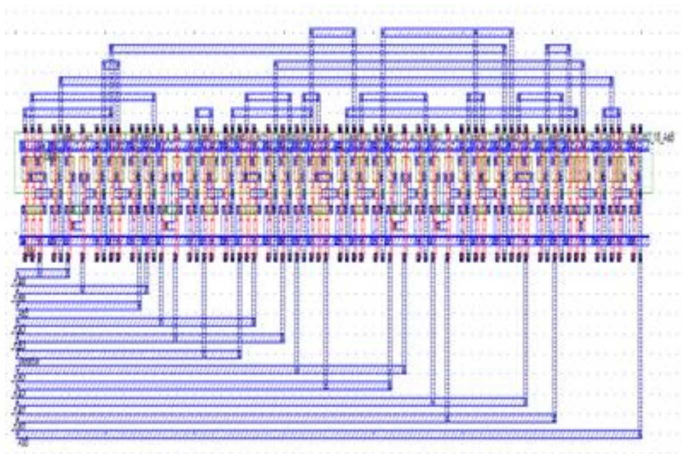


Fig.4.2. Layout of 4-bit conventional comparator

In similar way we can design 8-bit comparatorwhich is shown in fig.4.3.

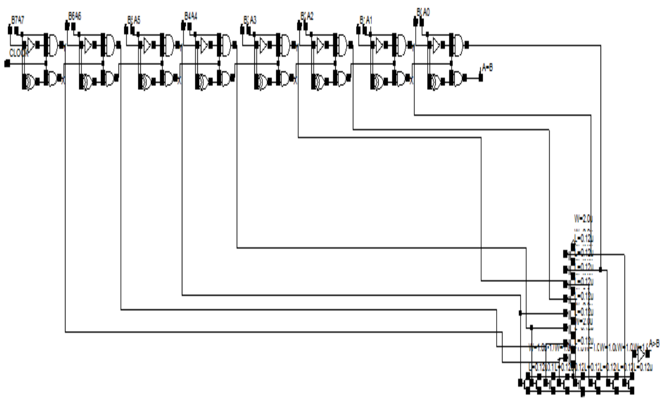


Fig.4.3.Schematic of8-bit conventional comparator

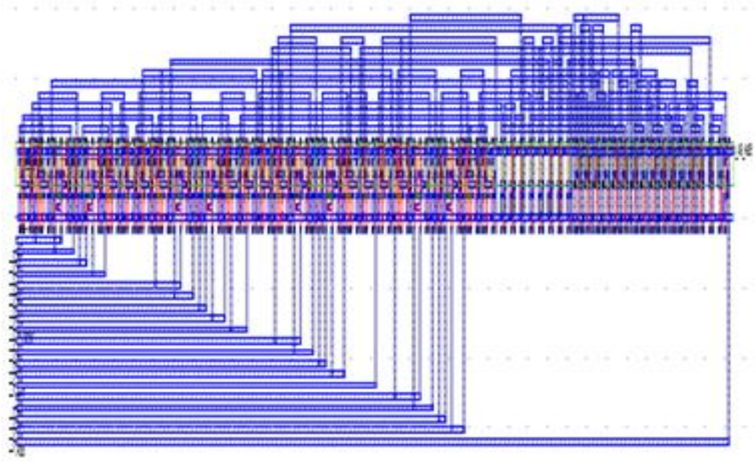


Fig4.4.Layout of 8-bit comparator

V. Design Of 8-Bitcomparator (Proposed)

The proposed comparator design consists of a precharged gate with 8pull-down stages connected to 7 intermediate pass-transistors, During the precharge period, (when the clock is low) each stage is precharged to VDD. In the evaluate period, (when the clock is high) the ithpull-down stack in the circuit will form a discharge path if Ai > Bi. The XNOR gates attached to the intermediate pass-transistors allow pull-down stack i - 1 to discharge the output if Ai = Bi. The XNOR gate outputs are computed during the precharge period to avoid any potential race condition caused by the pass transistors being in the wrong state. The result is that the output discharges if and only if A > B. Therefore, the output is high if and only if A > B. To determine A = B, the outputs of all the XNOR gates are ANDed together.

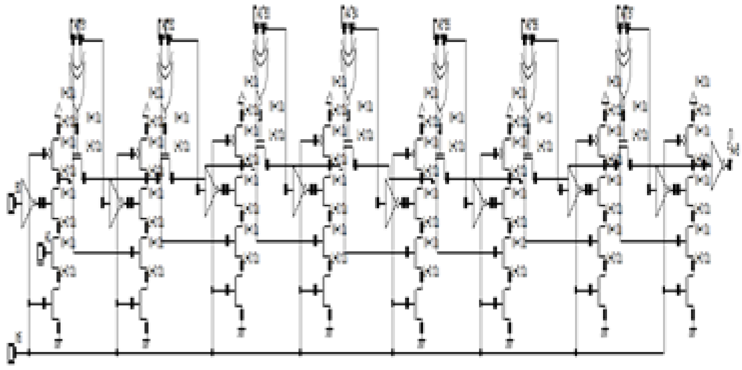


Fig.5.1. Schematic of 8-bit comparator (proposed)

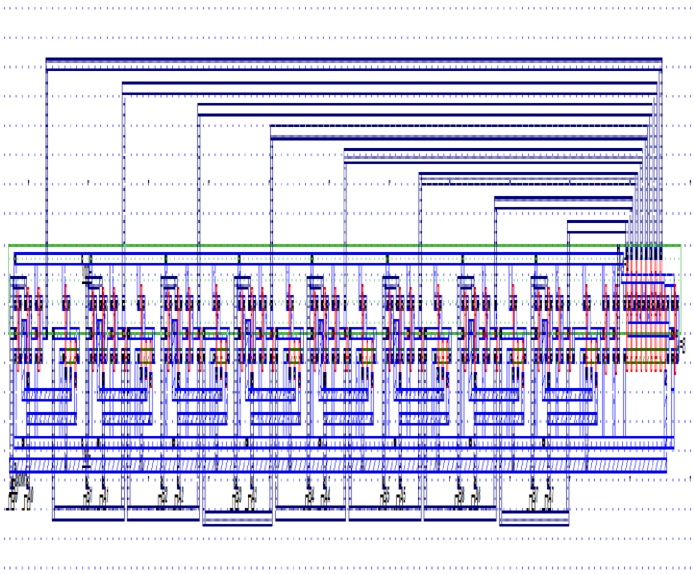


Fig.5.2. Layout of 8-bit comparator (proposed)

VI. Result And Discussion

At the precharged period (clock is deactivate i.e. low) each stage is precharged to VDD. But when clock is high 8th pull-down stack in the circuit will generate discharged path if Ai >Bi.The waveform of 8-bit comparator is shown in fig.6.1.

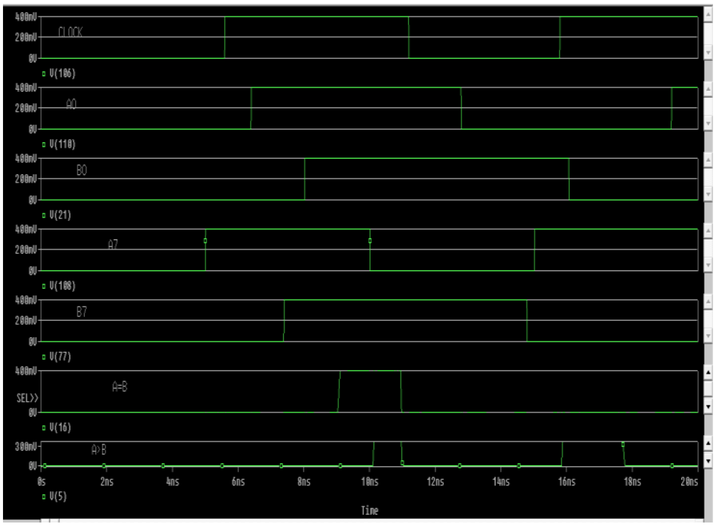


Fig.6.1. Waveform of 8-bit comparator (proposed)

So we can say that the output is low (if and only ifA<=B).The output becomes high when input A becomesgreater than input B.

Bits	No of transistors	Execution Time	Power Dissipation(watts)	Area$(\mu m)^2$
1	20	0.06	1.32E-12	10.21
4	90	0.16	2.61E-12	68.94
8	178	0.69	8.53E-12	165.16

Table: 6.1Simulation Result for conventional Comparator

Bits	No of transistors	Execution Time	Power Dissipation(watts)	Area$(\mu m)^2$
1	14	0.08	1.15E-12	7.41
4	59	0.30	4.94E-12	45.14
8	111	0.55	9.54E-12	104.34

Table: 6.2 Simulation Result for 8-bit comparator (proposed)

VII. Conclusion

This paper has described different designs for CMOS binary comparator and show different parameter like area, power, execution time and number of transistor. This design needs less area and less number of gates.CMOS circuit is used to construct the comparator by using the logic relation between different input and output. A Karnaugh map is used to minimize the representation of function..

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