Tranformerless H6 Grid Tied Inverter For Photovoltaic Generation

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Abstract: Transformer less inverter is widely used in grid-tied photovoltaic (PV) generation systems, due to the benefits of achieving high efficiency and low cost. Various transformer less inverter topologies have been proposed to meet the safety requirement of leakage currents, such as specified in the VDE-4105 standard. In this paper, a family of H6 transformer less inverter topologies withlow leakage currents is proposed, and the intrinsic relationship betweenH5 topology, highly efficient and reliable inverter concept(HERIC) topology, and the proposed H6 topology has been discussedas well. One of the proposed H6 inverter topologies is takenas an example for detail analysis with operation modes and modulationstrategy. A universal prototype is built for H6 topology mentionedfor evaluating their performances in terms of power efficiency and powerquality characteristics. Experimental results show that inthe proposed H6 topology, it has been found that with the increase in the switching frequency, the magnitude of higher order harmonics increases and that of lower order harmonics reduces. The size and cost of filter reduces as the order of harmonics increases, so a tradeoff must be done between the switching frequencies and the cost of filter the system

I. Introduction

The Photovoltaic generation is extensively increasing, since it is an essential inexhaustible and broadly available energy resource. For economic development of any country, energy is one of the critical inputs. Now a day's most of the energy is generated with fossil fuels which are non-renewable and cause environmental degradation by emission of carbon dioxide and other greenhouse gases, which are harmful to the environment. This has paved the way for research on renewable energy technology and other researches in the fields of power electronics and hence, the cost of utilizing the renewable energy is at an ever decreasing rate [1].

PV cells have an advantage of being maintenance and pollution free, but the cost of installation is high and in most of the power application they require a power converter for load interference. Also PV modules have relative low conversion efficiency. The overall system cost can be reduced by using high efficiency power converter[2]. Rapid advancement in the technology which extends from the field of renewable energy generation to the power supply of a portable digital device, impose great challenges on power electronics. The need of high efficiency, power density and reliability of power supply forcing power electronics engineers and researchers to find new way of power conversion with high efficiency and low losses. Ideally zero losses are aimed. But it is impossible to have lossless systems. Hence the power converters evolved from the earlier high loss, large linear power supplies to today's highly efficient and compact converters. In highly competitive industrial environment designers strive for improvement in efficiency, size and weight. In the recent past, various different inverter topologies have been proposed and are currently utilized for low power, singlephase grid-connected photovoltaic (PV) systems. A full-bridge inverter in combination with a line-frequency transformer is a familiar and common topology [3]. The transformer, however, is not a necessity or requirement and inverters avoiding transformers provide various advantages. Inverters without transformers outmatch those with presence of transformers with respect to higher efficiency, reduced cost, weight, embodied energy and minuscule size. When transformer is not used in the topology there is no method of increasing the inverter output voltage V_{inv} to the required RMS grid voltage value. Therefore, high DC bus voltage is required to guarantee the power flow from the PV array to the grid [3]. The system can only function when the DC bus voltage is more than the total amplitude of the grid voltage at all time. This constraint decides the minimum power rating of the system.

1.1 Common Mode Voltage Description

The common mode voltage of any circuit is the average of the voltages between the outputs and a common reference.

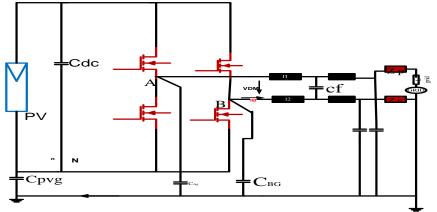


Fig: 1 Full Bridge Grid Tied Inverter

For the full-bridge inverter topology shown in Fig: 1.5 the negative terminal of the DC bus's point N is used as common reference. Therefore, the common-mode voltage, V_{cm} is given as: $V_{CM} = \frac{V_{AN} + V_{BN}}{2}$ (1.1)

$$I_{cm} = I_A + I_B = C_{PVg} \frac{dVcm}{dt}$$
(1.2)

The differential mode output voltage , V_{dm} is the voltage between both outputs : $V_{dm} = V_{AN} - V_{BN} = V_{AB}$

Combining equations (1.1) and (1.3) we get

$$V_{AN} = \frac{Vdm}{2} + V_{cm}$$
 (1.4)
 $V_{BN} = \frac{-Vdm}{2} + V_{cm}$ (1.5)

In addition to the common-mode voltage V_{cm} , two other sources, V_1 and V_2 are generated due to the asymmetries in the differential mode impedances [9][11]. Therefore, it is possible to have common-mode currents if any impedance asymmetry exists.

Inverters are the most important power electronics equipment in grid tied PV systems. Inverter interfacing PV modules with the grid ensures that the PV modules are operated at the maximum power. Their major role is to convert DC power into AC power. Based on the photovoltaic arrays output voltage, output power level and applications, the photovoltaic grid-connected system can adopt different topologies. These configurations describe the evolution of grid-connected inverters as from past, present and future technologies. There are different technologies and topologies available for transformer-less grid connected PV systems. In PV plants applications, various technological concepts are used for connecting the PV array to the utility grid. Each technology has its advantage and/or disadvantages compared to other, in terms of efficiency and power quality.

II. H5 Topology

The principle of H5 inverter topology can be explained with the help of fig: 2.1. It consists of five switches. And there are four operation modes in each period of the utility grid of the H5 topology, as shown in fig: 2.2. It can be seen that in the active modes, the inductor current of H5 topology is always flowing through three switches due to its extra switch S5 in dc side. In the freewheeling modes, the inductor current of H5 topology is flowing through two switches.

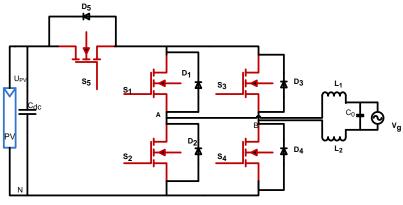


Fig: 2 H5 Topology

(1.3)

The basic operation of H5 inverter is illustrated by means of Fig: 3. Here all the four modes of operation of H5 inverter topology can be seen. During mode one gate pulses are given to switches S1, S4 and S5. When these switches are turned on there will be positive voltage V+ across the output end of the inverter. The direction of flow of current (clock wise) is as shown in the above Fig: 3.

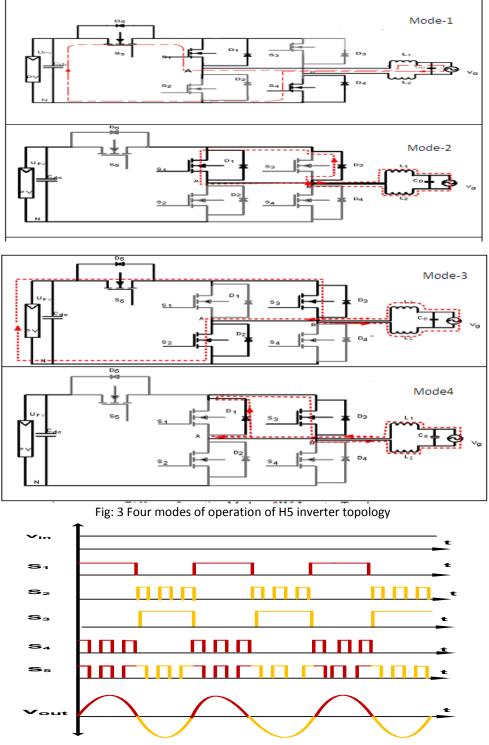
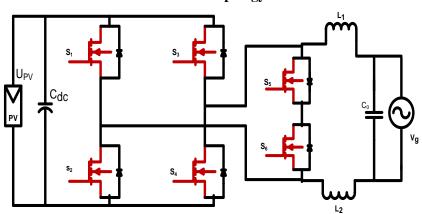


Fig: 4 Switching waveforms of H5 Inverter Topology

Figure two of the Fig 3 shows the second mode of operation of the H5 inverter, in the second mode gate pulse is given only to switch S1. This mode of operation is the first freewheeling mode. In the third mode of operation gate pulses are given switches S2, S3 and S5. When switches S2, S3 and S5 are turned on the direction of flow of current reverses (anti- clock wise) as shown in the Fig: 3 and the output voltage will be -V.

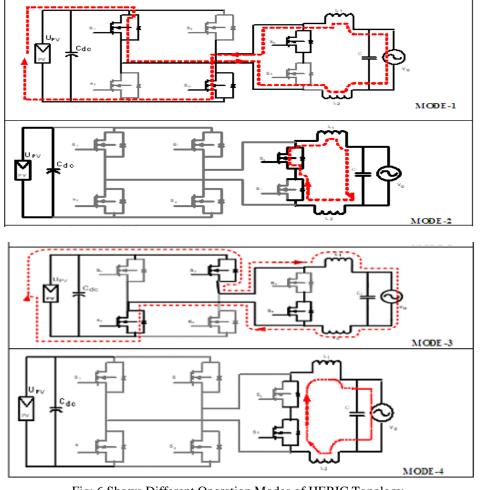
Finally in the fourth mode the $(2^{nd}$ freewheeling mode) during this mode gate pulse is only given the 3^{rd} switch hence the energy stored freewheels through the switch S3 and diode D1. Here we can see that during both the active modes switch S1 is kept on.



III. Heric Topology

Fig: 5 HERIC Topology

The above Fig: 5 show HERIC topology, the basic operation of HERIC inverter is illustrated by means of Fig 6. Here all the four modes of operation of HERIC inverter topology can be seen. In the first mode of operation gate pulses are given to switches S1, S4 and S5. When these switches are turned on there will be positive voltage V+ across the output end of the inverter. The direction of flow of current (clock wise) is as shown in the above Fig 6. The waveforms of the gate drive signals for HERIC topology are shown in Fig: 7.



Here it can be seen that there are six switches in this topology, even though gate pulses are given to three switches in the active mode, inductor current flows only through two switches, so on state losses are reduced to some extent as the conduction loss of one switch is reduced.

Figure two of the Fig: 6 shows the second mode of operation of the HERIC inverter, in the second mode, gate pulse is given only to switch S5. This is the first freewheeling mode, here the stored energy flows through switch S5 and the diode D6. In the third mode of operation gate pulses are given switches S2, S3 and S6. When switches S2, S3 and S5 are turned on the direction of flow of current reverses (anti- clock wise) as shown in the Fig: 6 and the output voltage will be -V. Finally in the fourth mode the (2nd freewheeling mode (dissipate) during this mode gate pulse is only given to 6th switch. Hence the energy stored freewheels through the switch S6 and diode D5.

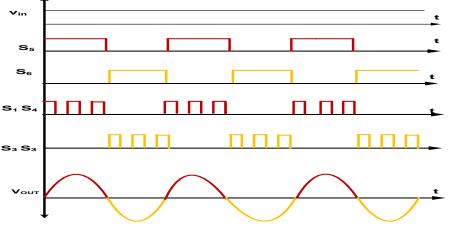


Fig:7 Switching waveforms of HERIC Inverter Topology

The above waveforms show the operation of HERIC topology; here we can see that during first active mode switches S_1 , S4, S5 are conducting.

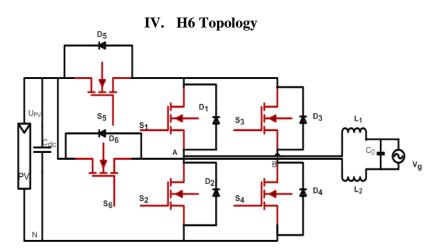


Fig: 8 Transformer-Less H6 Grid Tied Inverter Topology

The circuit structure of Transformer-less H6 grid tied inverter topology is shown in Fig: 8. From the aforementioned analysis, an extra switch *S*6 is introduced into the H5 inverter topology between the positive terminal of the PV array and the terminal (B) to form a new current path. As a result, a novel H6 transformer-less full-bridge inverter topology is derived.

There are four operation modes, as shown in Fig: 9. In the first mode of operation switches S1,S4 and S5 are given gate pulse, this is the first active mode of operation a positive voltage V+ across the output end of the inverter is obtained. In the second mode of operation switch S1 is left on and all the other switches are kept off. This mode is the first freewheeling mode; the energy stored is freewheeled through diode D3 and switch S1.

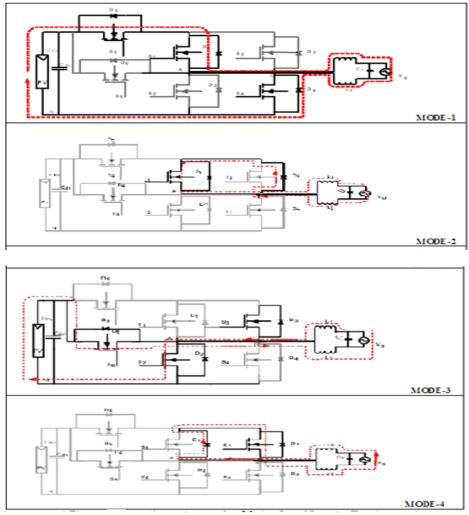


Fig: 9 Shows Different Operation Modes of H6 Inverter Topology

In the third mode of operation switches S2, S3 and S6 are given gate pulse the other switches are turned OFF. The inductor current is flowing through S2 and S6. Although S3 is turned ON, there is no current flowing through it, and the switch S3 has no conduction loss in this mode.Nevertheless, in the H5 topology, the inductor current flows through S2, S3 and S5. Therefore, the conduction loss of proposed topology is less than that of H5 topology, this is the second active mode of operation, and a voltage (V-) across the output end of the inverter is obtained. In the last mode of operation switch S3 is left on and all the other switches are kept off. This mode is the second freewheeling mode; the energy stored is freewheeled through diode D1 and switch S3.

Based on the above mentioned analysis, the PV array can be disconnected from the utility grid when the output voltage of the proposed H6 inverter is at zero voltage level and the leakage current path is cut off. The CM voltage of the proposed topology in each operation mode is equals to $0.5 U_{PV}$, and it results in low leakage current characteristic of the proposed H6 topologies. The proposed H6 topology with unipolar SPWM method not only can achieve unity power factor, but also has the ability to control the phase shifts between voltage and current waveforms. The drive signal is in phase with the grid-tied current. Therefore, it has the capability of injecting or absorbing reactive power, which meets the demand for VDE-4105 standard.

V. Hardware Implementation

After all the studies and design process the prototype of the H6 grid tied inverter is developed. The layout of the prototype developed is as shown in the Fig: 10. The switches used in the inverter are MOSFETs having part number IRF540N. To generate gating pulses a 16 bit RENESAS microcontroller (RL78_R5f102aa) is used and TLP 250 is used as gate driver.



Fig: 10 Hardware implementation of H6 inverter

VI. Experimental Results

Developed prototype is tested under various conditions. Main objective is to study the behavior of the inverter under various switching frequencies and duty cycle, and to check the amount of harmonics it injects into the system. To judge the quality of voltage generated by the inverter, a detailed harmonics analysis of voltage waveform is done. The following Fig: 11 show the Experimental setup of H6 inverter circuit for measurement of harmonics. The plot of harmonics for different duty cycle and switching frequencies are plotted. Output Voltage $V_0 = V_{IN} \times Duty$ cycle (5.1)

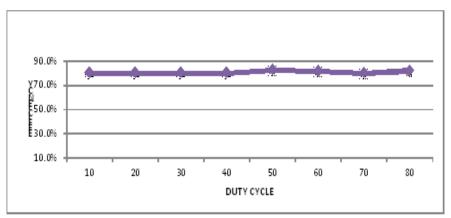
Efficiency =
$$\frac{V_{0 \text{ practical}}}{V_{0 \text{ ideal}}} \times 100 (5.2)$$



Fig: 11 Experimental setup of H6 inverter circuit for measurement of harmonics

| Sl no | Duty cycle | Input voltage | Output voltage | Efficiency | Switching Frequency | THD |
|-------|------------|---------------|-------------------|------------|------------------------|------|
| 1 | 10 % | 15 V | 1.2 | 80% | 1Khz | 19.0 |
| 2 | 20 % | 15V | 2.4 | 80% | 1Khz | 19.1 |
| 3 | 30 % | 15V | 3.6 | 80% | 1Khz | 19.2 |
| 4 | 40 % | 15V | 4.8 | 80% | 1Khz | 19.3 |
| 5 | 50 % | 15V | 6.2 | 82.6% | 1Khz | 19.4 |
| 6 | 60 % | 15V | 7.4 | 81.6% | 1Khz | 19.6 |

| Table I showing THD at different | duty cycle for | H6 topology |
|----------------------------------|----------------|-------------|
|----------------------------------|----------------|-------------|



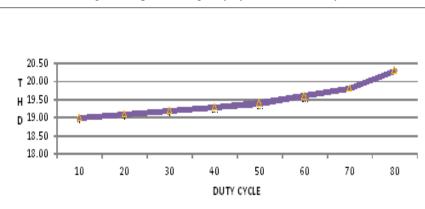


Fig: 12Graph showing duty cycle v/s. efficiency

Fig: 13 Graph showing duty cycle v/s THD

| Table II showing harmonics at different frequencies for H6 | topology |
|--|----------|
|--|----------|

| S | Switchin | Input | Out | Duty | 3 rd | 5 rd order | 7 rd order | 9 rd order | 11 rd | %TH | %los |
|---|----------|-------|-------|-------|-----------------|-----------------------|-----------------------|-----------------------|------------------|------|------|
| 1 | g | volta | put | cycle | order | harmoni | harmoni | harmoni | order | D | ses |
| n | frequenc | ge | volta | | harm | CS | CS | CS | harmo | | |
| 0 | У | | ge | | onics | | | | nics | | |
| 1 | 500 Hz | 15V | 7.6 | 60% | 17% | 5% | 4% | 2% | 1% | 19.6 | 15.5 |
| 2 | 1KHz | 15V | 7.5 | 60% | 15% | 6% | 5% | 5% | 2% | 19.4 | 16.6 |
| 3 | 2khz | 15V | 7.4 | 60% | 12% | 11% | 4% | 5% | 2% | 19.3 | 17.7 |
| 4 | 5khz | 15V | 7.2 | 60% | 7% | 12% | 7% | 7% | 2% | 19.1 | 20.0 |
| 5 | 10khz | 15V | 7.1 | 60% | 5% | 4% | 17% | 7% | 2% | 19.0 | 21.1 |
| 6 | 15khz | 15V | 7.0 | 60% | 2% | 1% | 4% | 17% | 4% | 18.6 | 22.2 |
| 7 | 20khz | 15V | 6.9 | 60% | 1% | 1% | 3% | 5% | 17% | 18.6 | 23.3 |

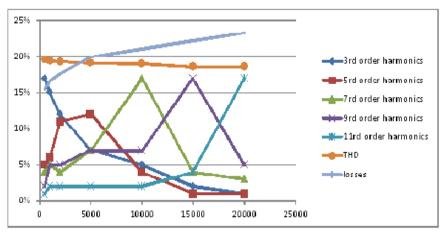


Fig: 14 showing comparison between different harmonicsat different switching frequencies

VII. Conclusion

The increased penetration of renewable energy sources into the power grid will help ease our dependence on fossil fuel-based energy sources. This paper is focused on the design of the PV-grid connected inverter power stage that supports the proposed PV system. In this project various grid tied inverters were studied and a H6 grid tied inverter is modeled. The behavior of grid tied inverter circuit is studied under different duty cycle and switching frequency. A H6 inverter is designed and to study the various properties of the converter the prototype of rating V_o = 12V, V_{in} =15V and f_s =10000 Hz was developed. It has been found that with the increase in the switching frequency, the magnitude of higher order harmonics increases and that of lower order harmonics reduces. The size and cost of filter reduces as the order of harmonics increases, but with high switching frequency, switching losses in the inverter increases, so a tradeoff must be done between the switching frequencies (efficiency) and the cost of filter the system.

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