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Design, Simulation and Implementation of Flyback based, True Single Stage, Isolated, Power Factor Corrected AC-DC Converter for Solar Arrav Simulators

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***ABSTRACT**: Presently most of the Power Factor correction circuits are based on boost topology. They consist of two stages, one being the power factor correction (pre-regulator) and later DC-DC conversion stage. This paper presents the design of a true single stage, isolated, power factor corrected, 110V-3.5A AC-DC converter as front end of Solar Array Simulators [7]. Flyback topology is used to achieve power factor correction as well as DC regulation in single step, and thus it simplifies two stage structure down to single stage. Single stage power factor corrected AC-DC converter has many advantages in term of cost and power density.*

***Keywords:** Power factor, AC-DC Converter, Solar Array Simulator, Harmonics*

I. INTRODUCTION

Power can be divided mainly into 3 forms:-

1. **True Power** which is measured in Watts and it is a function of dissipative elements (R).
2. **Reactive Power** which is measured in VAR and it is a function of reactive elements (X).
3. **Apparent Power** which is measured in VA and it is a function of total impedance (Z).

Power factor is a dimensionless quantity which can be defined as the ratio of the real power flowing to the load to the apparent power input to the circuit. More physically, power factor measures how efficiently the current is being converted into real power. For eg. A circuit with power factor of 0.7, the apparent power required by the circuit will be 1.4 times the real power used by the load.

Power simulators required in any satellite checkout are Battery simulators, Battery chargers and Solar Array Simulators. All these power simulators use front end AC-DC converters. If conventional AC-DC converters are used, their power factor will be poor and associated problems like current spikes which lead to imminent EMI/EMC problems.

From the instrumentation point of view, the term power factor basically consists of two components namely [2]

1. Displacement Power Factor (DPF).
2. Harmonic Power factor(HPF)

The True Power Factor (TPF) of any system is product of both of them.

TPF = DPF * HPF

Presently, boost converter based Power Factor Corrected (PFC) AC-DC converters are popular, whose block diagram [2] is shown in figure-1

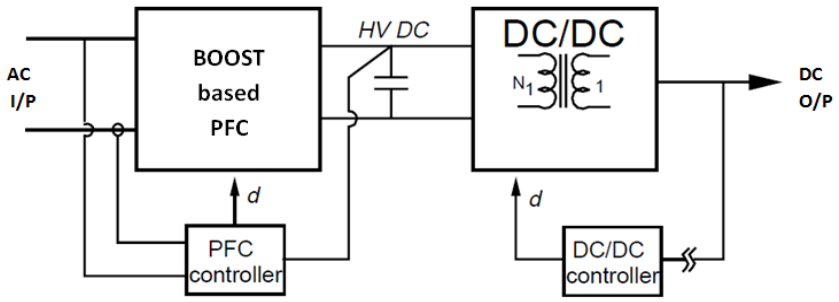

Fig. 1 Conventional two-stage AC-DC Converter

The paper presents the design, simulation and hardware implementation of true single stage, isolated PFC AC-DC converter. Flyback converter is used to simplify the two stage front end design to a single isolated PFC conversion stage, by integrating the PFC stage with the DC-DC conversion stage. Additionally the isolation is inherent to fly back converter. The single stage fly-back PFC design offers the following advantages:-

1. Reduction in component count and size.
2. Inherent isolation in the design.

Basic conceptual block diagram of the single stage is shown in figure-2

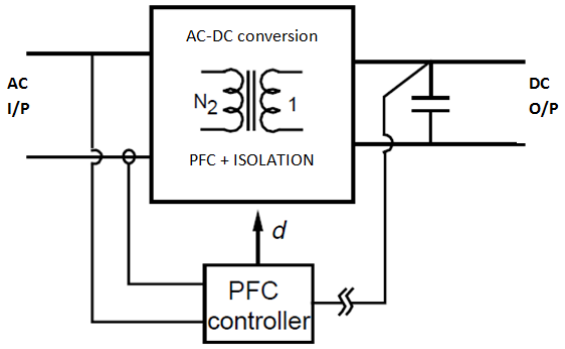

Fig. 2 Conceptual block diagram of single stage AC-DC converter

II. SINGLE STAGE ARCHITECTURE

The single stage architecture is divided into two parts:-

1. O/P Voltage regulation Loop :-

This loop is an outer loop which maintains DC output voltage. It sets the reference for the inner current loop by multiplying the output of the first loop with incoming scaled down sinusoidal signal. A linear isolator is used to isolate the feedback (Output voltage) from the secondary ground. A isolated feedback voltage and reference is fed to the error amplifier, which generates error signal. The variation in the outer loop changes the magnitude of the current drawn from the mains.

2. Power factor correction and current loop :-

The inner control loop is the one, which implements Power factor correction and output voltage control, by modulating the ON and OFF times of the semiconductor switch. The reference for this loop is from the multiplier. The current feedback is derived from a current sense resistor which is in series with line of AC supply. The magnitude of the multiplier output will decide magnitude of the line current and the shape of the multiplier output will dictate the phase and shaping of the line current.

Functional block diagram of single stage AC-DC converter architecture is shown in figure 3

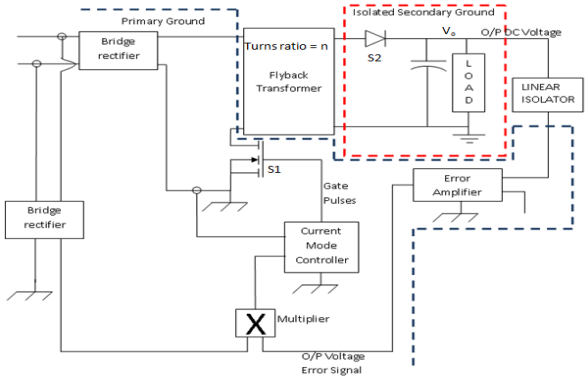

Fig. 3 Functional block diagram of single stage, flyback converter based AC-DC converter

III. DESIGN REQUIREMENTS

Design inputs:

1.	Input AC voltage	:	230V ± 10%.
2.	Input AC Frequency	:	50 ± 2 HZ.
3.	Output ripple Voltage	:	1V.
4.	Output Voltage (Vo)	:	110V DC.
1.	Output Current	:	0.5 – 3.5A DC.
2.	Switching Frequency	:	20KHz
3.	No. of Stages	:	Single Stage

Determination of Fly-back transformer turns ratio:

The optimum turns ratio of fly-back transformer is selected considering the voltage stress on switches S1 and S2 (refer figure 3).

Let Vs1 be the voltage stress on switch S1 (MOSFET) placed on the primary side. It consists of two terms,

1. Vin max
2. Reflection of output voltage on the primary side which can be given by (Vo/n)

Thus voltage stress on switch S1 can be given as

$$Vs1 = Vin\ max + \left(\frac{Vo}{n}\right), \text{ ---------- (1)}$$

Where,

V_{S1} is the voltage across the MOSFET,
$V_{in\ max}$ is the maximum input voltage to the chopper,
Vo is the output DC voltage,
n = (N_2/N_1)Turns ratio of fly-back transformer/coupled inductor
Similarly, let Vs2 be the voltage stress on the switch S2 (diode) placed on the secondary side, and it is given as

$$Vs2 = Vo + (Vin\ max * n), \text{ ---------- (2)}$$

Where,
V_{s2} → Reverse voltage stress (PIV) across the secondary rectifier diode
Using the above equations the computed values of voltage stress is given in the table below.

Stress on switch S1 Vs1(V)	Stress on switch S1 Vs2(V)	Total stress (Vs1 + Vs2) (V)	N2/ N1
907.8	181.6	1089.4	0.2
724.4	217.3	941.7	0.3
632.7	253.2	885.9	0.4
577.7	288.9	866.6	0.5
541.1	324.7	865.8	0.6
514.9	360.5	875.4	0.7
495.3	396.2	891.5	0.8
480	432.0	912	0.9
467.7	467.8	935.5	1

Table 1 Voltage Stress on S1 (MOSFET) and S2 (Diode)

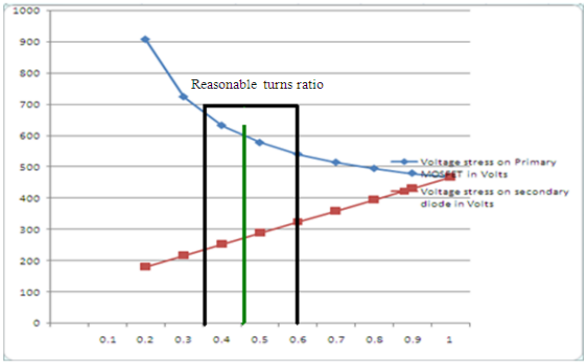

Fig. 4 Stress Vs Turns Ratio

Figure 4 shows the stress on individual semiconductor switches. It can be noted that the stress on S1 (primary MOSFET) reduces exponentially turns ratio. Whereas the stress on S2 (output diode) increases linearly with turns ratio. Table 4 shows the total stress (Vs1 + Vs2) is minimum for turns ratio of 0.4 to 0.6. Thus based on simplicity of design, n = 0.5 is chosen.

Calculation of Minimum Duty cycle (Dmin):
We have

$$Vo = n * Vin\ max * \left(\frac{D}{1-D}\right) \text{ ---------- (3)}$$

At maximum input AC voltage duty cycle will be minimum, therefore from eq. (3) we can have

$$Vo = \left[n * Vin\ max * \left(\frac{Dmin}{1-Dmin}\right)\right]$$

$$110 = \left[0.5 * 253 * \left(\frac{Dmin}{1-Dmin}\right)\right]$$

We get D*min* = 0.464 or 46.4%
Therefore minimum duty cycle is 46% i.e. $[(50 * 10^{-6}) * 0.464] = 0.23\mu s.$
Determining the value of the primary inductance (Lp) and secondary Inductance of fly-back transformer (Ls)
We have,

$$L_p = \frac{V_o * D}{\Delta I_L * f_s} \text{ ---------- (4)}$$

Where,
L_p → Primary inductance

$V_0 \rightarrow$ Output DC voltage
$\Delta I_l \rightarrow$ Output ripple DC current
$f_s \rightarrow$ Switching Frequency

Therefore the value of the primary inductance will be

$$L_p = \frac{110 * 0.464}{0.5 * 20 * 10^3}$$
$$L_p = 5.104 \text{ mH.}$$

For secondary inductance
We have the relation,

$$\frac{N_1}{N_2} = \sqrt{\frac{L_p}{L_S}}$$
$$L_S = L_p * \left(\frac{N_1}{N_2}\right)^2$$
$$L_S = 2.552 \text{ mH.}$$

Calculation of the primary peak current and secondary peak current:
Secondary current:
We have the relation,

$$I_0 = \left(\frac{I_{S-} + I_{S+}}{2}\right) * (1 - D) \text{ ---------- (5)}$$

Substituting the values of the corresponding terms we get,

$$3.5 = \left(\frac{I_{S-} + I_{S+}}{2}\right) * (1 - 0.46)$$

Thus,

$$(I_{S-} + I_{S+}) = 12.96 \text{ A.} \text{ ---------- (6)}$$

Equating the energy stored in the inductor we get,

$$P_O * T_S = \left(\frac{1}{2}\right) * L_S({I_{S+}}^2 - {I_{S-}}^2)$$

Substituting the values we get,

$$770 * 50 * 10^{-6} = 2.552 * 10^{-3} * 12.96 * (I_{S+} - I_{S-})$$

On solving the above equation we get,

$$(I_{S+} - I_{S-}) = 1.164 \text{ A.} \text{ ---------- (7)}$$

We also have the relation,

$$I_{S+} = \left(\frac{I_O}{1 - D}\right) + \left(\frac{V_O * (1 - D)}{2 * L_S * f_S}\right)$$

And

$$I_{S-} = \left(\frac{I_O}{1 - D}\right) - \left(\frac{V_O * (1 - D)}{2 * L_S * f_S}\right)$$

Solving eq. (5), (6), (7) , we get,

$$I_{S+} = 7.069 \text{ A.} \text{ ---------- (8)}$$
$$I_{S-} = 5.891 \text{ A.} \text{ ---------- (9)}$$

Similarly for primary current we have,

$$I_{p+} - I_{p-} = \left(\frac{V_I * D}{L_p * f_S}\right) \text{ ---------- (10)}$$

Substituting the values we will get,

$$I_{p+} - I_{p-} = 1.14 \text{ A} \text{ ---------- (11)}$$

Again equating the energy stored in the inductor we get,

$$P_O * T_S = \left(\frac{1}{2}\right) * L_p * (I_{p+} - I_{p-}) * (I_{p+} + I_{p-})$$

Thus we get

$$(I_{p+} + I_{p-}) = 6.616\ A \text{---------- (12)}$$

For input current we have,

$$I_{in} = \left(\frac{I_{p+} + I_{p-}}{2}\right) * D$$

Thus, solving eq. (8), (9), (10)

$$I_{in} = 1.521\ A.$$

$$I_{p+} = \left(\frac{I_{in}}{D}\right) + \left(\frac{V_i * D}{2L_p * f_s}\right)$$

$$I_{p+} = \left(\frac{1.521}{0.46}\right) + \left(\frac{253 * 0.46}{2 * 5.104 * 10^{-3} * 20 * 10^3}\right)$$

$$I_{p+} = 3.876\ A. \text{---------- (13)}$$

$$I_{p-} = \left(\frac{I_{in}}{D}\right) - \left(\frac{V_i * D}{2L_p * f_s}\right)$$

$$I_{p-} = \left(\frac{1.521}{0.46}\right) - \left(\frac{253 * 0.46}{2 * 5.104 * 10^{-3} * 20 * 10^3}\right)$$

$$I_{p-} = 2.736\ A. \text{---------- (14)}$$

Calculation of output filter capacitance (Co):

Using the specification of the output voltage ripple we can calculate output capacitance(Co),

$$C_o = \frac{I_o * (1 - D)}{\Delta V_o * f_s}$$

Substituting the values we get,

$$C_o = \frac{3.5 * (1 - .46)}{0.3 * 20 * 10^3}$$

$$C_o = 31.5\ mF$$

IV. SIMULATION

The proposed circuit topology is simulated in SIMULINK/MATLAB. The figure 5 below shows the simulink model of single stage fly back PFC circuit with simple ON-OFF control. The results are shown in the subsequent figures. The Total Harmonic Distortion of the input current is also analyzed.

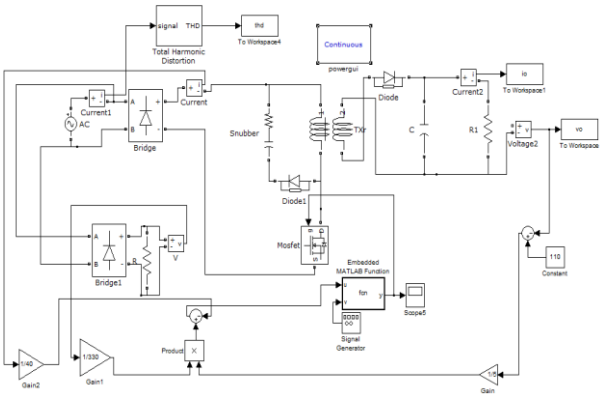

Fig. 5 SIMULINK Block diagram

V. SIMULATION RESULTS

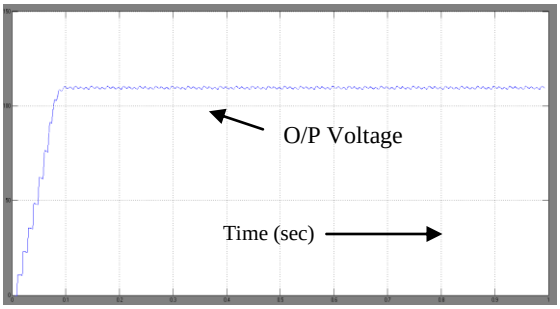

Fig. 6 O/P Voltage

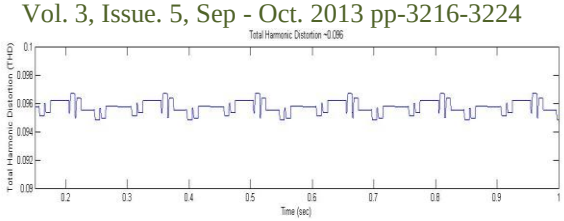

Fig. 7 Total Harmonic Distorion (THD)

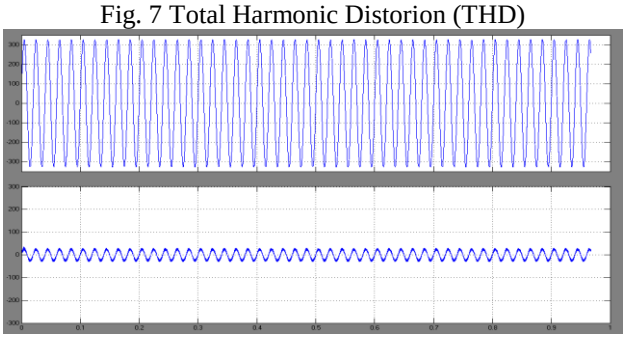

Fig. 8 I/P voltage and I/P current

VI. HARDWARE RESULTS

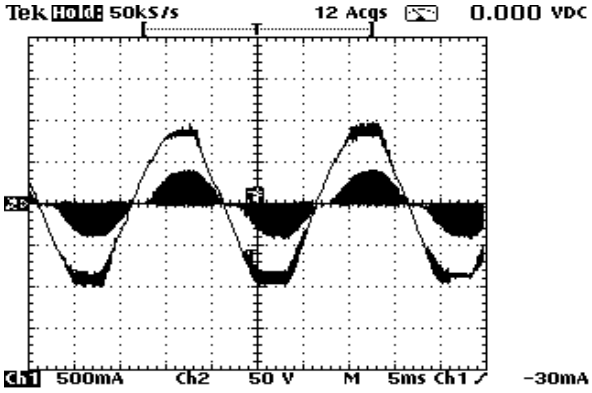

Fig. 9 (a) Open Loop Output of the flyback converter

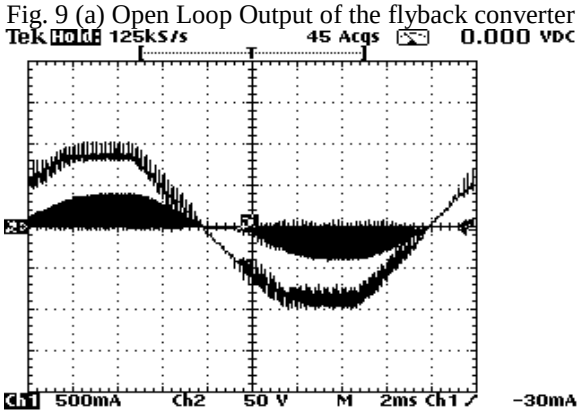

Fig. 9(b) Open Loop Output zoomed

Figure 9 (a)&(b) show the open loop output of the flyback converter. It is observed that the current is delayed w.r.t voltage by around 1.8milisecond which corresponds to a Displacement Power Factor of 0.87.

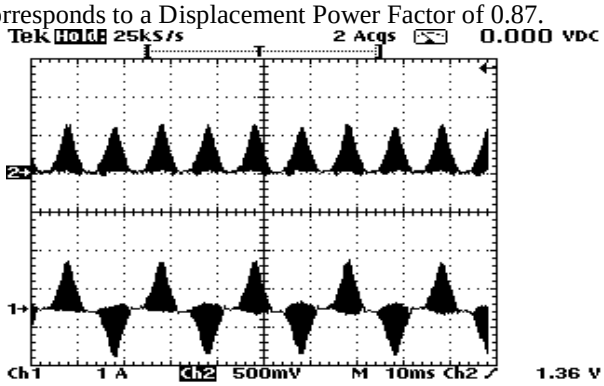

Fig. 10 Input current reference

In the above figure 10, channel 1 shows the actual input current and channel 2 shows the input current reference to the current mode controller IC.

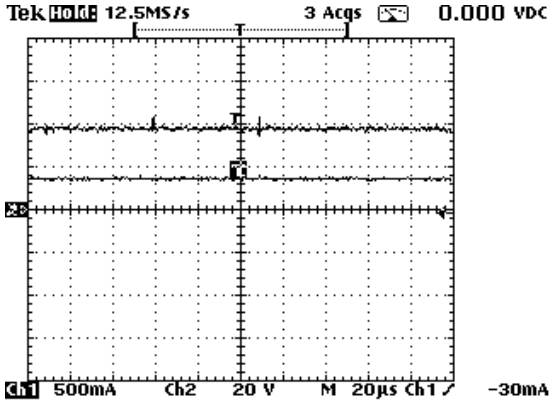

Fig. 11 Output voltage and current

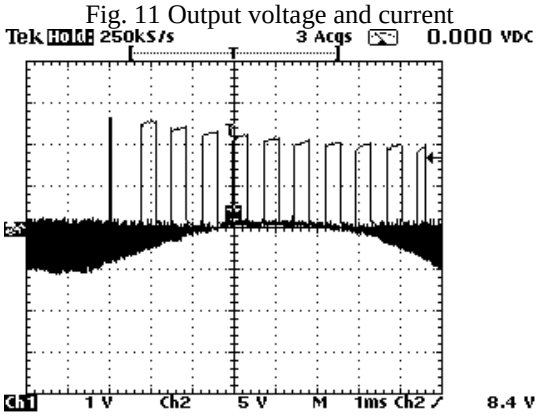

Fig. 12 Duty cycle variation with current feedback

Figure 12 shows the variation of the PWM duty cycle variation with respect to the input current variation. It is observer that at lower current the duty cycle is maximum and it reduces as the current reference becomes higher.

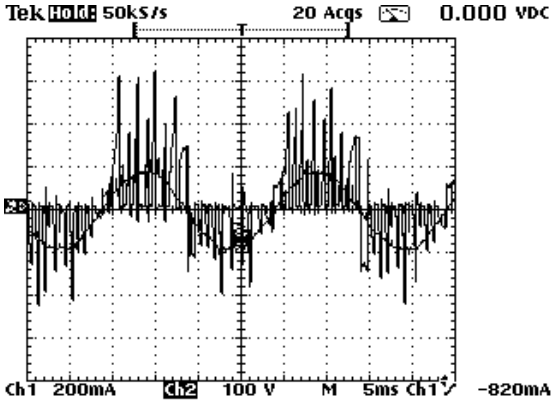

Fig. 13 Input current vs Input voltage

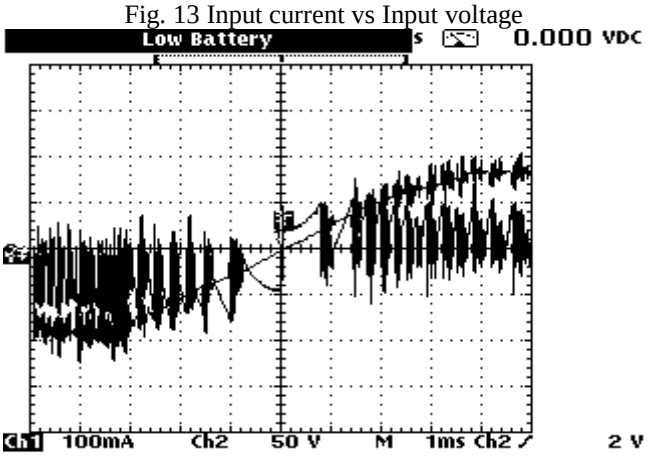

Fig. 14 Displacement between I/P current and I/P voltage

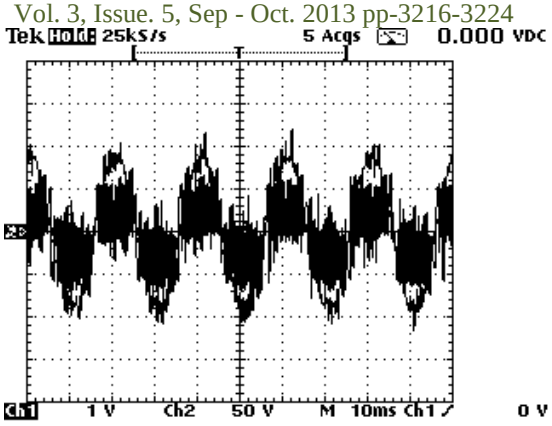

Fig. 15 I/P voltage vs I/P current

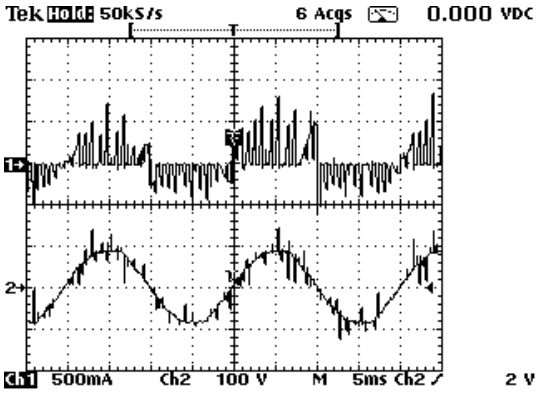

Fig. 16 I/P voltage vs I/P current

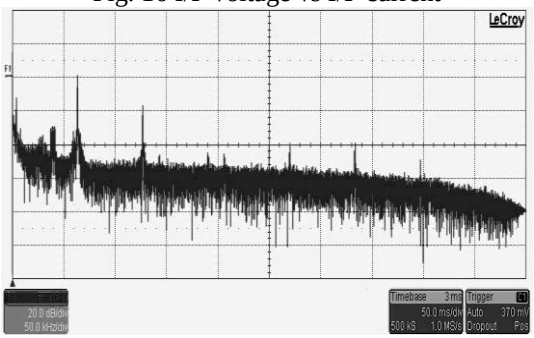

Fig. 17 FFT of the I/P current (switching component)

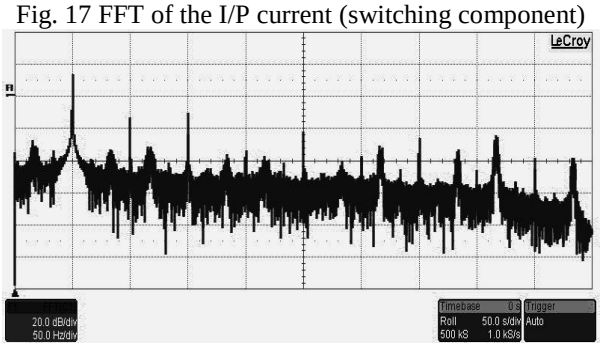

Fig. 18 FFT of the I/P current (Fundamental and its components)

VII. DISCUSSION

Simulation results shows that the Displacement power factor of the circuit is equal to 0.99 and the Total harmonic distortion is near 0.09. Thus the Harmonic power factor (HPF) can be calculated as,

HPF = 1/[sqrt (1+ (THD^2))]

HPF = 0.995

Displacement Power Factor = 0.99

True Power Factor = 0.99*0.995 = 0.98

Practically, the displacement power factor is improved to 0.99. The figures 17 and 18 shows the FFT of the I/P current. From the FFT, the Total Harmonic distortion was found to be 1%.

Thus the Harmonic power factor was also improved to 0.99, which results in true power factor of 0.98.

VIII. CONCLUSION

The design of a true single stage, isolated, power factor corrected,110V-3.5A AC-DC is successfully completed and simulated using SIMULINK-MATLAB®. A power factor of 0.98 is achieved in simulation model.
Practically a single stage Power Factor Corrected 40V-2A AC-DC converter is designed and developed using suitable components and the displacement power factor was improved from 0.87 to 0.99. The harmonic power factor is also considerably improved. The final achieved power factor is 0.98 which is very close to unity.

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