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Scan-Based Delay Measurement Technique Using Signature Registers

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ABSTRACT: *With the scaling of semiconductor process technology, performance of modern VLSI chips will improve significantly. However, as the scaling increases, small-delay defects which are caused by resistive-short, resistive-open, or resistive-via become serious problems. The proposed method uses a signature analysis and a scan design to detect small delay defects. The proposed measurement technique measures the delay of the explicitly sensitized paths with the resolution of the on-chip variable clock generator. The proposed scan design realizes complete on-chip delay measurement in short measurement time using the proposed delay measurement technique and extra latches for storing the test vectors.*

Index terms: Very large scale integration (VLSI), signature register, design for testability (DFT).

I. INTRODUCTION

Semiconductor process technology has developed rapidly to improve the performance of modern VLSI chips. As a continuous process scaling produces large-scale chips. With the rapid development of semiconductor technology, delay testing has become a critical problem. The major types of delays are occurred because of resistive-shorts, resistive-open and resistive-vias. These small delays can cause a fail of a system if they are activated for a longer time. Furthermore their life time become very short. Therefore to overcome these drawbacks some embedded delay measurement techniques have been proposed. Scan-based delay measurement technique with variable clock generator is one of these on-chip delay measurement techniques. The delay of path is measured by continuous sensitization of path under measurement with test clock width reduced gradually. The advantage of this technique is its high accuracy. This technique has some drawbacks. Therefore we present a scan-based delay measurement technique which uses signature registers.

A.EXISTING SYSTEM

These days, various methods for small-delay defect detection have been proposed. Scan-based delay measurement technique with variable clock generator is most widely used. In this technique the delay of path is measured by continuous sensitization of path under measurement with test clock width reduced gradually by resolution. In this technique the accuracy is high. The reason of the high accuracy is that the technique measures just the period between the time when a transition is launched to the measured path and the time when the transition is captured by the flip flop connected to the path, directly. The variation of the measured value just depends on the variation of the clock frequency of the clock generator. Therefore, if the clock generator is compensated the influence of the process variation, the measured value does not depend on the process variation.

B. DRAWBACKS OF EXISTING SYSTEM

Disadvantages of existing system are as follows.

- The gap between the functional clock and scan clock frequency increases. Therefore the measurement time becomes too long to make it practical.
  Area reduction technique of the self testing scan-FFs is also proposed. The flip flop reduces the required number of scan operations, which makes the measurement time practical.
- However, the area overhead of these methods is still expensive compared with the conventional scan designs.

C. PROPOSED SYSTEM

We present a scan-based delay measurement technique using signature registers for small-delay defect detection. The proposed method does not require the expected test vector because the test responses are analyzed by the signature registers. The overall area cost is of the order of conventional scan designs for design for test (DFT). The measurement time of the proposed technique is smaller than conventional scan-based delay measurement. The extra signature registers can be reused for testing, diagnosis, and silicon debugging.

D. ADVANTAGES OF PROPOSED SYSTEM

- Proposed method does not require expected test vectors.
- The measurement time is smaller.

- The overall area cost is of the order of conventional scan designs for design for test (DFT).

E. VARIABLE CLOCK GENERATOR

In the proposed method, the clock width should be reduced continuously by a constant interval. It is difficult for an external tester to control this clock operation. Therefore an on-chip variable clock generator is used for the proposed method. In this paper, we use the on-chip variable clock generator. Figure1 illustrates the circuit. The circuit consists of the arbitrary clock frequency generator and the 2-pulse generator. The arbitrary clock frequency generator generates an arbitrary clock width. The 2-pulse generator generates 2-pulse test clocks with arbitrary timing in response to a trigger signal.

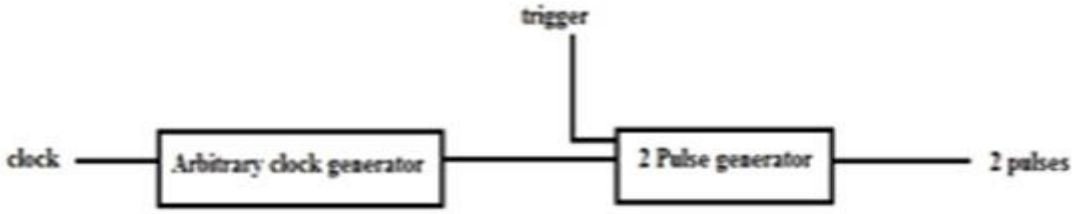


Figure 1: variable clock frequency generator

II.DELAY MEASUREMENT TECHNIQUE USING SIGNATURE REGISTER

The proposed measurement is scan-based delay measurement. The difference from the existing one is use of signature registers and additional latches. In this measurement latches are used to store test vector after scan-in operation.

A.SCAN FLIP FLOPS

An important flip-flop function for ASIC testing is so-called scan capability. The idea is be able to drive the flip-flop's D input with an alternate source of data during device testing. When all of the flip-flops are put into testing mode, a test pattern can be "scanned in" to the ASIC using the flip-flops' alternate data inputs. After the test pattern is loaded, the flip-flops are put back into "normal" mode, and all of the flip-flops are clocked normally. After one or more clock ticks, the flip-flops are put back into test mode, and the test results are "scanned out. Figure2 shows the gate level description of scan flip flop. The lines D, Q, and clk are the input, output, and clock lines, respectively. When se0=0, the flip flop is in normal operation mode. When se0=1 and se1=1, the flip flop is in scan operation mode. When se0=1, se1=0, the flip flop loads the value stored in the latch connected to the latch line. The lines si and s0 are the input and output for constructing the scan path.

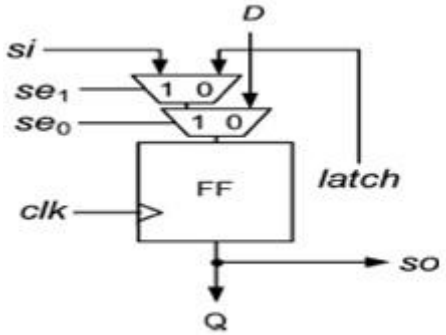


Figure 2: scan flip flop

B.RECONFIGURABLE SIGNATURE REGISTER

Signature analysis registers are often used in combination with standard LFSRs for on-chip self test of VLSI circuits. The signature register for the proposed measurement requires the following functions to meet the demand of the proposed measurement.

• Capturing the test response in arbitrary timing.
• Shifting out the signature data in arbitrary timing.

Figure3 shows the architecture of the signature register for the proposed measurement. It has four flip flops FF0, FF1, FF2, and FF3. . When sge = 1 , it works as a signature register. When sge=0, it works as a shift register. The line in is the input of the signature register. The clock line is controlled by sck . When sck = 0 , the signature register does not capture the input value. When sck = 1 , the signature register captures the input value synchronizing with the positive edge of clk . By controlling sck, the signature registers capture only the target test response. The output is sg0. The measurement system requires multiple signature registers generally.

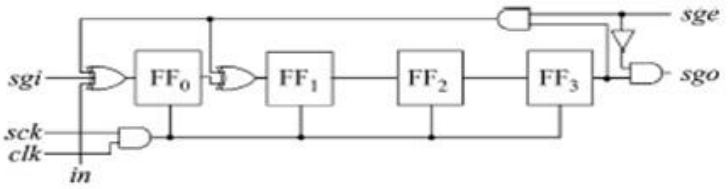


Figure3: 4- bit reconfigurable signature register

III.DELAY MEASUREMENT SYSTEM

Delay measurement system is shown figure 4. The proposed system consists of the low cost tester and the chip with the variable clock generator (VCG) explained in and a BCD decoder. The chip is assumed to have single functional clock in the proposed method, and the chip has two reset lines for initializing the flip flops and the signature registers independently. The reset operations are controlled by the tester. The low cost tester controls the whole measurement sequence. The clock frequency tck is slower than the functional clock. The line sg0 retrieves the signature data from the signature registers to estimate the measured delay. The line sci sends the test vectors to the scan input of the chip. The line sc0 gets the data of the flip flops from the scan output of the chip. In the proposed measurement sequence, sc0 is not used. However, it is used to check the flip flops or the additional latches before the measurement. The line cs is the clock control line. The proposed measurement uses both the slow tester clock tck and the fast double pulse generated by on-chip VCG. The line selects the slow and fast clock. If cs is 1, the fast clock is sent to the clock line clk of the components. Otherwise the slow tester clock tck is sent. The lines trg and cnt are the input lines for VCG. The fast double pulse is launched synchronizing with the positive edge of trg . The line cnt controls the width of the double pulse. The line se controls the scan flip flops. The line lck controls the latches for storing test vectors. The lines scj_0, scj1…..scj_{l-1} are the inputs for the encoded data to control the capture operation of the signature registers. The BCD decoder decodes the encoded input data to the control data of the signature registers sck0…sck_{m-1}. As explained later, the decoder is used to reduce the input lines for the control data of the signature registers. The sge is the enable signal for the signature registers. The control lines of the signature registers are connected to the BCD decoder.

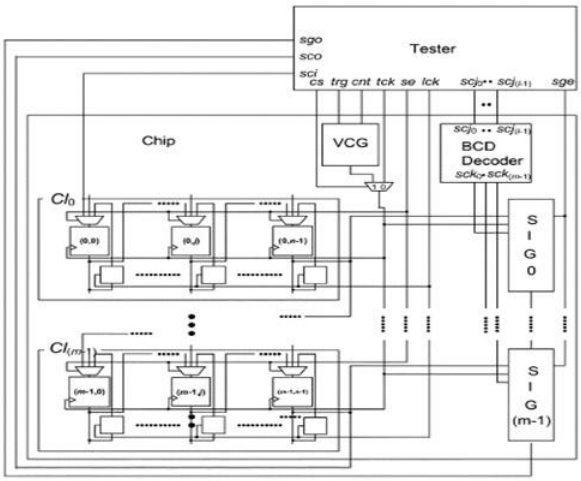


Figure 4: measurement system

A. MEASUREMENT SEQUENCE PER TEST VECTOR

When the measurement system has m signature registers, m paths can be measured in parallel maximally. The measurement strategy using the example is depicted in figure5. In this example, the proposed method consists of six flip flops FF_0-FF_5.the flip flops are classified to the two clusters cl_0 andcl_1. Each cluster has its own signature register $SIG_0$and SIG_1 respectively. The pathsp_1, p_2, p_3 , p_5 are sensitized by the test vector $(FF_0, FF_1, FF_2, FF_3, FF_4, FF_5)$ = (0, 0, 1, 0, 1, 1).The test response ofp_i, is captured byFF_i. The expected test response is $(FF_0, FF_1, FF_2, FF_3, FF_4, FF_5) = (1,1,0,1,0,0)$. The paths p_1 and p_2 are measured by SIG_0. The paths $p_3$and p_5 are measured by SIG_1. The combination of two paths, one of which is selected from p_1 andp_2, the other which is selected from p_3 and p_5, can be measured simultaneously. First, the test vector is set to the flip flops with scan-in operation. After that, the values of flip flops are set to extra latches. Second, the first stage is performed. Third the second stage is performed. In each stage, the paths under measurement are tested multiple times with reducing test clock width. Steps (b) and (c) show the state after test execution. The flip flops hold the test response. The latches hold the test vector. After testing, the responses are shifted to signature registers with clock operation ofclk. The number of required shift clocks varies in each stage.

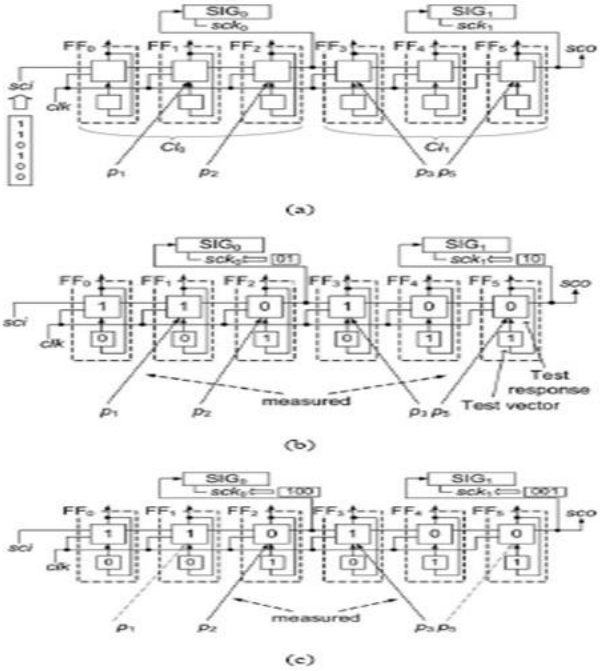
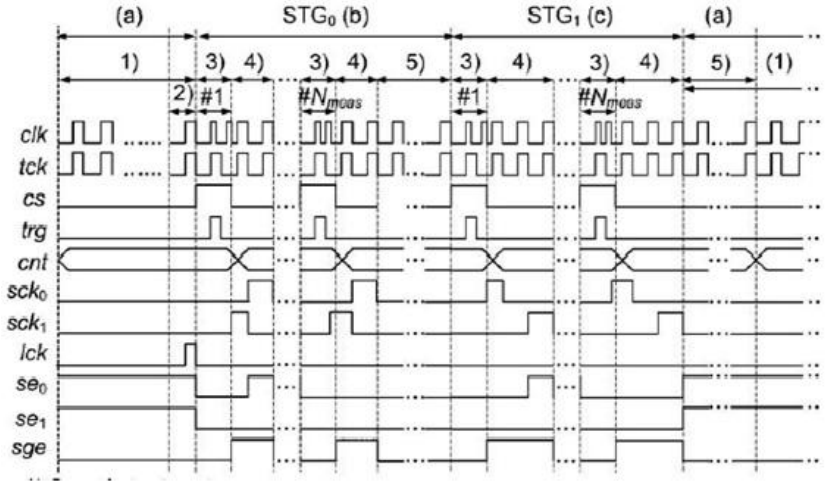


Figure 5: measurement of paths sensitized in attest vector in parallel. (a) scan-in test vector and store it in latches. (b) Sending test responses of p_1 and p_5 to SIG_0 andSIG_1. (c) Send test responses of p_2 and p_3 SIG_0 and SIG_1.

Figure6 shows the timing chart of operation. The low cost tester controls the whole measurement sequence. For measurement both VCG clock and tester clock are used. The clock controlled by cs. The triggered signal trg and control signal cnt are provided to VCG. The control data cnt is updated after each testing operation. In STG_0, SIG_0 captures the test response in second shift-out clock. Therefore sck_0 turns to 1 synchronizing with the negative edge of first clock of the shift-out operation. The latch clock lck captures the value of the flip flops just after scan-in operation is finished.



1) Scan-in test vector.
2) Set initial vector to L_j.
3) Apply test clock.
4) Transfer test responses to signature registers.
5) Retrieve signature data.

Figure 6: timing chart of the sequence of figure5.

B.WHOLE MEASUREMENT SEQUENCE

Let us assume that the test set for measurement TS has N_{TV} test vectors$tv_0, \ldots . tv_{NTV-1}$. The number of stages of tv_i is$N_{st(i)}$. Before measurement, we have to check if the flip flops, the latches, and the clock generator work correctly by applying test vectors. After that the following measurement sequence is executed.

Step 1: Initialize the variable$i = 0$.

Step 2: if i is equal toN_{TV}, finish, otherwise initialize the variable j to0, and set tv_i to the flip flops with scan-in operation.

Step 3: send the values of flip flops to the latches.
Step 4: the paths included in STG_j are measured simultaneously. After that, $j$is updated to $(j+1)$.
Step 5: if j equal to $N_{st(i)}$, go to step 6, otherwise load the test vector from the latches to flip flops, and go to step 4.
Step 6: i is updated to $i+1$, and go to step 2.

C.TESTER CHANNEL REDUCTION

If sck of each signature register is directly fed to the inputs of the chip, it requires the same number of extra inputs as the number of the signature registers. It increases tester channel width. To keep the tester channel width short, we use BCD decoder. The decoder circuit transforms n bit binary code in to the corresponding 2^n width decimal code. The example to encode sck bit sequences to the corresponding binary code is shown in figure7. It consists of three clusters $cl_0, cl_1,$ and cl_2. Each cluster has three flip flops. Consider the case that test response of sensitized paths are captured in $FF_{01}, FF_{12}, FF_{20}$.in the shift out operation after a testing, the test response of FF_{01} is captured by SIG_0 two clocks later. Therefore the bit sequence "010" should be sent to sck_0 .the test response of FF_{12} is captured by SIG_1 one clock later. Therefore the bit sequence "100" should be sent to sck_1 . The test response of $FF_{02}$is captured by SIG_2 three clocks later. Therefore bit sequence "001" should be sent to sck_2. Each bit value of this bit sequence is grouped. The group of 0^{th} bit value is $sck_0 sck_1 sck_2 = 010$. Those of first bit values and second bit values are $sck_0 sck_1 sck_2 = 100$, $sck_0 sck_1 sck_2 = 001$, respectively. We call each group slice. Here, sl_i represents the slice of i^{th} bit. Finally the decimal codes are transformed to binary code. The 0^{th} slice sl_0 "010" is transformed to "10". The 1^{st} slice sl_1 "100" is transformed to "10". The second slice sl_2 "001" is transformed to "11". As a result the bit width of data is reduced from 3 bit to 2 bit by transformation. Generally, the width of the slice of sck is n, the width of encoded slice of scj is $[log_2 n]$. However, for the encoding, each slice is permitted only 1 bit with the value 1. More than two bits with the value are not permitted.

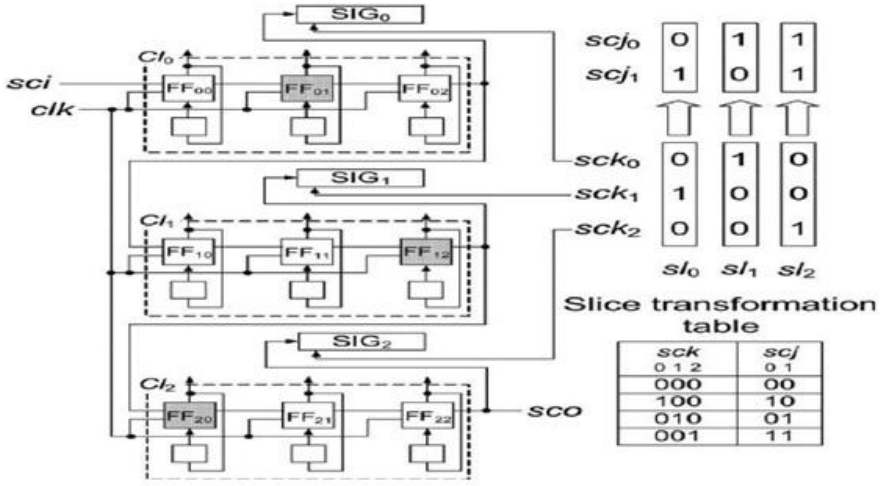


Figure 7: encoding the output data of BCD decoder

D.TEST RESPONSE TRACING

The target paths of proposed measurement are single-path sensitizable. In single path sensitizable measurement, it is guaranteed that once the test fails the test with higher frequency than the failing frequency is fail. Let L_{SIG} be the length of the signature register, the measurement sequence of a path with test response tracing mode is described as follows.
Step1: SIG is initialized.
Step2: Test vector is loaded from the latches.
Step3: Test clock width T is set to normal clock width.
Step4: Test clock is applied.
Step5: The test response is sent to SIG with scan-out operation.
Step6: If testing is equal to N_{meas} or multiple number of L_{SIG} , the values of flip flops of SIG is retrieved. After that, if testing time is equal to N_{meas} , go to step 7, otherwise go back to step 2after the test clock width T is updated to $T - \Delta T$.
Step 7: The delay value is estimated by comparing the retrieved signature value and the signature table.

IV.SIMULATION RESULTS

In this section, on-chip path delay under different process variations will be simulated and measured. During the simulation we measure the delay of each path under test. Random faults were injected in circuits to generate erroneous data. Random input patterns were applied to the ISCAS-89 benchmark circuits and compared with proposed method. The length of the signature register is 8 bit. The test set consists of test vectors which detects all single-path sensitizable transition faults. The paths sensitized by these test vectors are measured. The measurement times using the proposed scan design and is calculated by Tsig =time required for {whole scan-in + double pulse + SIG data}

Simulation results of delay measurement using signature register are shown in figure8 and figure9

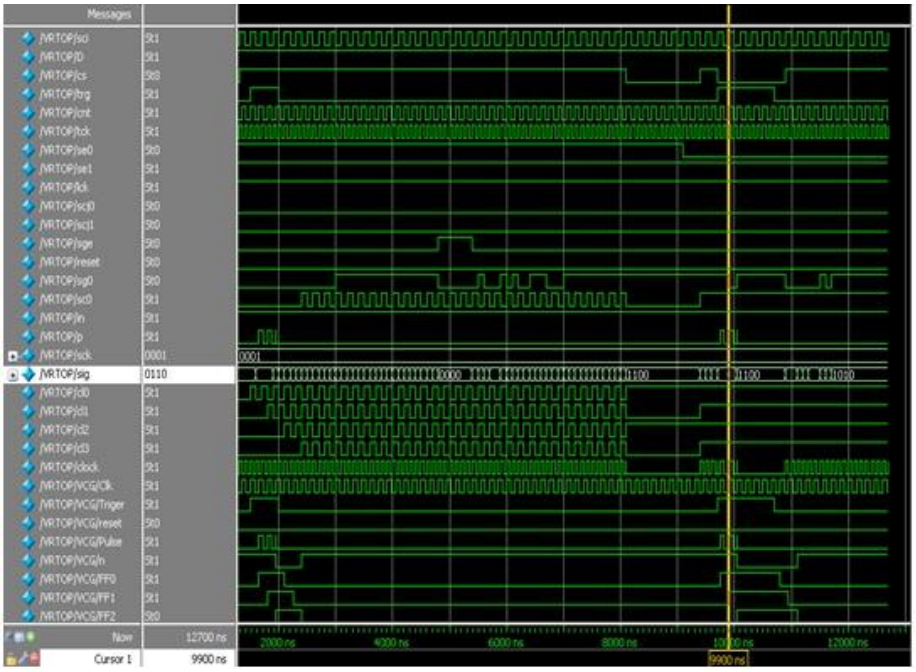


Figure 8: Simulation results

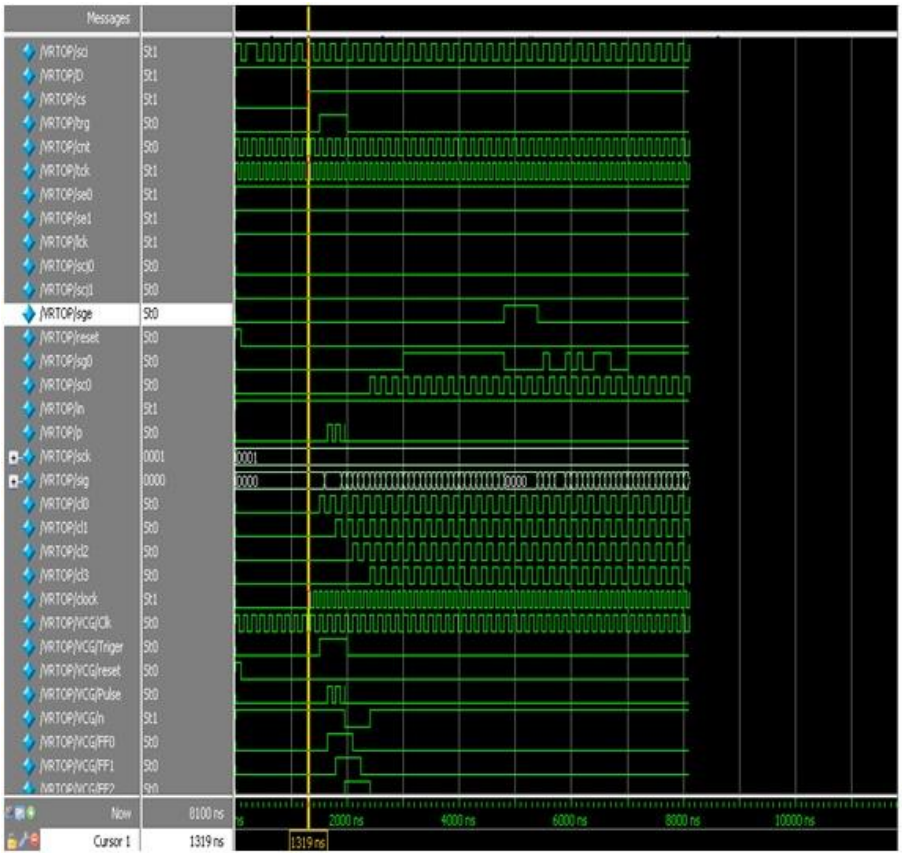


Figure9: simulation results

The device utilization summary for the delay measurement technique is shown in Table I

Logic utilization	*used*	*available*	*Utilization*
Total number of slice register	43	7,168	1%
Number used as flip flop	31		
Number used as latches	12		
Number of 4 input LUTs	47	7,168	1%
Number of occupied cells	47	3,584	1%
Number of slices containing only related logic	47	47	100%
Number of slices containing unrelated logic	0	47	0%
Number of 4 input LUTs	47	7,168	1%
Number of bonded IOBs	13	141	9%
Number of BUFGMUXs	3	8	37%
Average fan out non clock nets	2.76		

Table I: device utilization summary

CONCLUSION

• The proposal of the delay measurement method using signature analysis and variable clock generator.
• The proposal of a scan design for the delay measurement of internal paths of SOC.

The first proposal can be applied not only SOC but also field programmable gate array (FPGA). A future work is the low cost application of the proposed measurement to FPGA. When we measure short paths the measurement error can increase for the IR drop induced by higher test clock frequency. It can reduce the test quality. Another future work is the reduction and the avoidance of the measurement error caused by the IR drop.

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