A DER Based Single-Phase Asymmetrical 27 Level Inverter Topology

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ABSTRACT : *This paper deals single phase 27-level multilevel inverter topology for DER's-based DC/AC conversion system. This work mainly focuses on cascaded MLI using three unequal dc sources in order to produce twenty seven-level output. In this study, a high step-up converter is introduced as a front-end stage to improve the conversion efficiency of conventional boost converters and to stabilize the output dc voltage of DERs such as photovoltaic modules for use with the simplified MLI. A conventional 27-level cascade multilevel inverter requires a combination of 13 H-bridge (single-phase full-bridge) inverter modules but the present topology, 27 level multilevel inverter is obtained by using only 3 H-bridge inverter modules with different dc voltage sources This MLI offers strong advances such as improved output waveforms, smaller filter size, low THD, reduced volume and cost, and lower electromagnetic interference. The need of several sources on the DC side of the converter makes multilevel technology attractive for many photovoltaic applications. This paper provides an overview of DER based 27-level multilevel inverter topology and investigates their suitability for single-phase. A simulation model based on MATLAB/SIMULINK(version 7.12) is developed.*

Keywords: *Cascaded H Bridge inverter, High step-up converter, PV Array, THD.*

I. INTRODUCTION

Conventional energy systems and high-energy Factories located in the geographical locations suitable for the production of the majority of Power, which is then transported to the consumption of large Long-distance transmission lines to the center. System Control centers monitor and control the system continuously to ensure the quality of the power. For delivering premium electric power in terms of high efficiency, reliability, and power quality, integrating interface converters of DERs such as photovoltaic (PV), wind power, micro turbines, and fuel cells into the micro grid system has become a critical issue in recent years[1]-[4]. In such systems, most DERs usually supply a dc voltage that varies in a wide range according to Various load conditions. In light of public concern about global warming and climate change, much effort has been focused on the development of environmentally friendly distributed energy resources (DERs). Thus, a dc/ac power processing interface is required and is compliable with residential, industrial, and utility grid standards Multilevel inverters can be divided into three presentable topologies; diode-clamped, flying-capacitor, and cascaded H- bridge cell [5]-[9]. Among them, cascaded H-bridge multilevel inverters have been received a great attention because of their merits such as minimum number of components, reliability, and modularity. In the viewpoint of obtaining a sinusoidal output voltage multilevel inverters may increase the number of output voltage levels. However, it will need more components resulted in complexity and cost increase. To minimize these drawbacks, multilevel inverters employing cascaded transformers have been studied Owing to the trinary characteristic of output voltage, they can synthesize high quality output voltage near to sinusoidal waves. By using a cascaded transformer, they obtain galvanic isolation between source and loads. However, the transformer may decrease the power conversion efficiency, and volume and cost will be increased. To alleviate these problems, propose a cascaded H- bridge multilevel inverter using trinary dc input source without transformers [10].

In the case of photovoltaic (PV) systems, the grid connection of many small (less than 50 kW) specifically designed inverters can be anticipated. These generators will inevitably have some impact on the voltage waveform at the point of common coupling, and thus on the network power quality. When power-electronic sources are operated in parallel, two particular effects are apparent which affect harmonic generation: attenuation and cancellation (see [18] and [19]). Attenuation occurs since the generated currents cause voltage variations that in turn affect the other sources; the impact is such as to reduce the currents causing the disturbance. Cancellation is the result of the harmonic current components of the different sources being to some extent out of phase, resulting of course in a reduction in that particular harmonic for the aggregate. The specific case of cancellation of the switching harmonics for multiple inverters, which can generally be taken to be of statistically independent phase, has been dealt with in recently published work, [20]. The objective of this paper is to study a newly constructed transformer less 27-level Multistring inverter topology for DERs. In this work, proposed inverter is reduced to multilevel inverter topology that requires only twelve active switches instead of the fifty-two required in the conventional cascaded H-bridge (CCHB) multilevel inverter [21]. In addition, among them, two active switches are operated at the line frequency. The input to the proposed prototype is obtained from PV modules. In order to improve the conversion efficiency of conventional boost converters, a high step-up converter is also introduced as a front-end stage to stabilize the output dc voltage of each DER (PV) modules for use with the simplified multilevel.

II. PV ARRAY

PHOTOVOLTAIC (PV) power supplied to the utility grid is gaining more and more visibility, while the world's power demand is increasing [11]. Not many PV systems have so far been placed into the grid due to the relatively high cost, compared with more traditional energy sources such as oil, gas, coal, nuclear, hydro, and wind. Solid-state inverters have been shown to be the enabling technology for putting PV systems into the grid. Photons of light with energy higher than the band-gap energy of PV material can make electrons in the material break free from atoms that hold them and create hole- electron pairs. These electrons however, will soon fall back into holes causing charge carriers to disappear. If a nearby electric field is provided, those in the conduction band can be continuously swept away from holes toward a metallic contact where they will emerge as an electric current. The electric field with in the semiconductor itself at the junction between two regions of crystals of different type, called a p-n junction. The PV cell has electrical contacts on its top and bottom to capture the electrons. When the PV cell delivers power to the load, the electrons flow out of the n-side into the connecting wire, through the load, and back to the p-side where they recombine with holes [8]. Note that conventional current flows in the opposite direction from electrons.

2.1 Demands Defined by the Photovoltaic Cell(s)

A model of a PV cell is sketched in Figure. 1(a) and its electrical characteristic is illustrated in Figure.1 (b). The most common PV technologies nowadays are the mono crystalline and the multi crystalline-silicon modules, which are based on traditional, and expensive, microelectronic manufacturing processes [11]. The MPP voltage range for these PV modules is normally defined in the range from 23 to 38 V at a power generation of approximate 160 W, and their open-circuit voltage is below 45 V. However, new technologies like thin-layer silicon, amorphous-silicon, and photo Electro Chemical (PEC) are in development [11], [12]. These types of PV modules can be made arbitrarily large by an inexpensive "roll-on–roll-off" process.

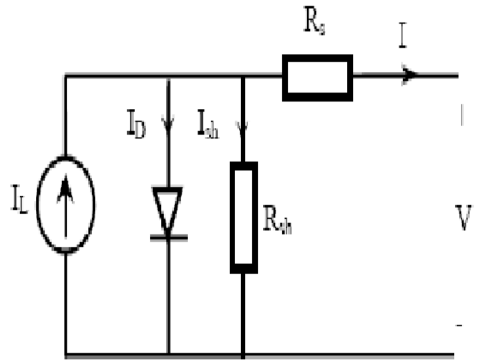

Fig 1 (a)

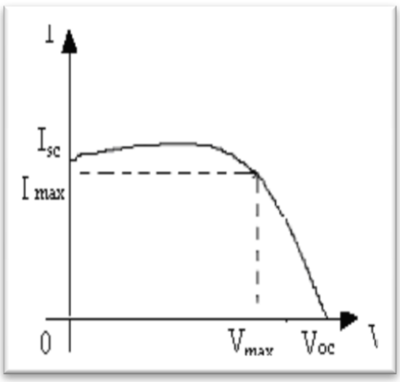

Fig 1 (b)

Figure. 1. Model and characteristics of a PV cell. (a) Electrical model with current and voltages defined.
(b) Electrical characteristic of the PV cell, exposed to a given amount of light at a given temperature.

As indicated, ripple at the PV module's terminals results in a somewhat lower power generation, compared with the case where no ripple is present at the terminals. This means that new modules with only one cell may see the light in the future. The voltage range for these cells/modules is located around 0.5, 1.0 V at several hundred amperes per square meter cell [13]–[15]. The inverters must guarantee that the PV module(s) is operated at the MPP, which is the operating condition where the most energy is captured. This is accomplished with an MPP tracker (MPPT). It also involves the ripple at the terminals of the PV module(s) being sufficiently small, in order to operate around the MPP without too much fluctuation. Analyses of the circuit in Figure. 1(a) shows that there is a relationship between the amplitude of the voltage ripple and the utilization ratio [16].A solar cell basically is a p-n semiconductor junction. When exposed to light, a current proportional to solar irradiance is generated. The circuit model of PV cell is illustrated in Figure.1 (a). Standard simulation tools utilize the approximate diode equivalent circuit shown in Figure.1 (a) in order to simulate all electric circuits that contain diodes**.**

2.2 Theoretical Mathematical Model

The equation [1] & [2] that are used to solve the mathematical model of the solar cell based on simple equivalent circuit shown in Figure. 1, are given below;

$$I_D = I_O \left[e^{\frac{q(V+IRs)}{KT}} - 1\right] \quad \ldots\ldots\ldots\ldots \quad (1)$$

$$I = I_L - I_O \left[e^{\frac{q(V+IRs)}{KT}} - 1\right] - \frac{V+IRs}{Rsh} \quad \ldots\ldots\ldots\ldots \quad (2)$$

Where:
I is the cell current in (A).
q is the charge of electron = 1.6x10-19 (coul).
K is the Boltzmann constant (j/K).
T is the cell temperature (K).
IL is the light generated current (A).
I_o is the diode saturation current.
Rs , Rsh are cell series and shunt resistance (ohms).
V is the cell output voltage (V).

Equation (1) was used in computer simulation to obtain the output characteristics of a solar cell, as shown in the Figure1(b). This curve clearly shows that the output characteristics of a solar cell are non linear and are crucially influenced by solar radiation, temperature and load condition.

2.3. Variation in Available Energy Due To Sun's Incident Angle:

PV cell output with respect to sun's angle of incidence is approximated by a cosines function at sun angles from 0° to 50° .Beyond the incident angle of 50° the available solar energy falls of rapidly as shown in the Figure 1. Therefore it is convenient and sufficient within the normal operating range to model the fluctuations in photocurrent (I_{ph}) verses incident angle is given by Equation (3)

2.4. Power Vs Voltage Characteristics:

Figure 2 shows the typical Power versus Voltage curve of the PV array. In this Figure, P is the power extracted from PV array and V is the voltage across the terminals of the PV array. The characteristics have different slopes at various points. When maximum power is extracted from PV array the system is operating at MPP where slope is zero. The PV curve varies according to the current insulation and temperature. When insulation increases, the power available from PV array increases whereas when temperature increases, the power available from PV Array decreases.

$$I_{ph} = I_{max} \cos\theta \quad \ldots\ldots\ldots\ldots \quad (3)$$

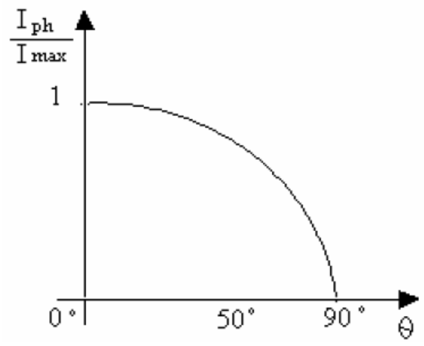

Figure 2: Power Vs Voltage

The graph shown in Figure.3 is used to find the maximum power extracted from the sun when the PV arrays are inclined a different angles. From the Figure we observe that Max power is obtained when the slope of the PV array is equal to zero.

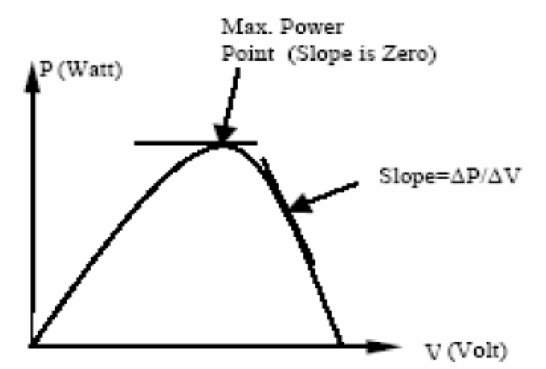

Figure. 3: Variation In Available Energy Due Sun's Incident Angle Variation.

III. HIGH STEP-UP CONVERTER STAGE

In this study, high step-up converter topology in [13] is introduced to boost and stabilize the output dc voltage of various DERs such as PV cell modules for employment of the proposed simplified multilevel inverter. The architecture of a high step-up converter initially introduced from depicted in Figure-4, and is composed of different converter topologies: boost, fly back, and a charge circuit.

The coupled inductor of the high step-up converter can be modeled as an ideal transformer, a magnetizing inductor and leaky inductor.

According to the voltage–seconds balance condition of the magnetizing inductor, the voltage of the primary winding can be derived as

$$Vpri = Vin.\frac{D}{(1-D)} \quad \ldots\ldots\ldots\ldots \quad (4)$$

where V_{in} represents each the low-voltage DC energy input sources, and voltage of the secondary winding is

$$Vsec = \frac{Ns}{Np}.Vpri = \frac{Ns}{Np}.Vin.\frac{D}{(1-D)} \quad \ldots.(5)$$

Similar to that of the Boost converter, the voltage of the charge-pump capacitor C pump and clamp capacitor Cc can be expressed as

$$Vcp = Vcc = Vin.\frac{D}{(1-D)} \quad \ldots\ldots\ldots \quad (6)$$

Hence, the voltage conversion ratio of the high step-up converter, named input voltage to bus voltage ratio, can be derived as

$$\frac{Vsi}{Vin} = (2 + \frac{Ns}{Np}.\frac{D}{(1-D)}) \quad \ldots\ldots\ldots\ldots \quad (7)$$

IV. NEW MULTILEVEL INVERTER

The new hybrid multilevel inverter consists of full bridge modules which have the relationship of 1v, 3v, 9v,…..3s-1V for dc link Voltage The output waveform has 27 levels, ± 13 V_{dc}, ± 12 V_{dc}, ±11 V_{dc} , ±10 V_{dc}, ± 9 V_{dc}, ±8 V_{dc}, ±7 V_{dc}, ±6 V_{dc}, ± 5 V_{dc}, ±4 V_{dc}, ±3 V_{dc}, ± 2 V_{dc}, ±1 V_{dc}, and 0.The inverter generates 3s different voltage levels (e.g.an inverter with S =3 cells can generate 3^3=27 different voltage level).The basic hybrid multilevel inverter structure for single phase is illustrated in Figure 4.This multilevel inverter is made up of a set of series connected cells. Each cell consists of a 4-switch H-bridge voltage source inverter. The output inverter voltage is obtained by summing the cell contributions. In conventional method, low level inverter is used. Better sinusoidal output was not obtained which is the drawback of the conventional system and the harmonics was high. So increase the levels of the inverter to get high resolution, hence the output wave form is mostly sinusoidal wave form. The common function of multilevel inverter is to synthesize a desired voltage from several separate DC sources [2]. Each source is connected to a single phase full bridge inverter. Each inverter is capable of generating three different output voltages, +V_{dc}, 0 and –V_{dc}.

4.1 Modeling Of New Multilevel Inverter:

For each full bridge inverter the output voltage is given by $V_{0i} = V_{dc}(S_{1i} - S_{2i})$

And the input dc current is $I_{dci} = I_a(S_{1i} - S_{2i})$

i =1, 2, 3… (Number of full bridge inverters employed). I_a *is* the output current of the new inverter. S_{1i} and S_{2i} is the upper switch of each full bridge inverter. Now the output voltage of each phase of the new multilevel inverter is given by

$$Von = \sum_{i=1}^{n} V0i$$

V. NEW THREE H-BRIDGE 27-LEVEL MULTILEVEL INVERTER

The topology of the proposed Dc–Ac H-bridge multilevel inverter is shown in Figure.4. The inverter uses a standard three-leg and an H bridge with its dc source in series with each phase leg.

In the proposed method of the inverter, there are three input stages. All the modules are connected as new hybrid with each module having power switches. The power switches may be IGBT, MOSFET or any other power devices. The MOSFET's are used in this system. The power switches are operated in switching mode such that any two switches are in operating conditions at a time and other two remain in open condition. The switching is as S_1=$S_3$and S_2= S_4. This method is adopted to protect the circuit from short circuiting. The number of levels is increased by connecting maximum number of modules.

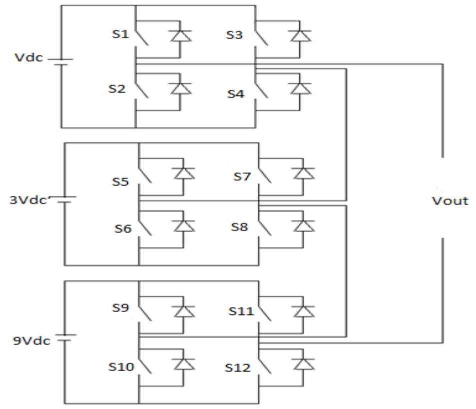

Figure 4: Single phase dc–ac three H-bridge 27 levels multi level inverter.

5.1 New Multilevel Inverter Switching:

Table.1 New Multi Inverter Switching Sequence

Output voltages and switching states for the new hybrid inverter, S=3																											
V dc	**Vout -13 v**	**-12 v**	**-11 v**	**-12 v**	**-9 v**	**-9 v**	**-7 v**	**-6 v**	**-5 v**	**-4 v**	**-3 v**	**-2 v**	**-1 v**	**0 v**	**1 v**	**2 v**	**3 v**	**4 v**	**5 v**	**6 v**	**7 v**	**8 v**	**9 v**	**10 v**	**11 v**	**12 v**	**13 v**
1v dc1	**N**	**O**	**P**	**N**	**O**	**P**	**N**	**O**	**P**	**N**	**O**	**P**	**N**	**O**	**P**	**N**	**O**	**P**	**N**	**O**	**P**	**N**	**O**	**P**	**N**	**O**	**P**
3v dc1	**N**	**N**	**N**	**O**	**O**	**O**	**P**	**P**	**P**	**N**	**N**	**N**	**O**	**O**	**O**	**P**	**P**	**P**	**N**	**N**	**N**	**O**	**O**	**O**	**P**	**P**	**P**
9v dc1	**N**	**N**	**N**	**N**	**N**	**N**	**N**	**N**	**N**	**O**	**O**	**O**	**O**	**O**	**O**	**O**	**O**	**O**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**

VI. PROPOSED CONCEPT

The proposed prototype consists of three stages of operation as shown in figure 5.First stage deals with DERs such as PV modules supply dc voltage that varies in a wide range according to various load conditions. In this paper three individual dc voltages 30V, 90V, 270V are obtained from three individual PV modules and then they are boosted to 100V, 300V, 900V respectively by using boost converter in the second stage of operation. In the third stage, boosted dc sources are applied as inputs to the proposed asymmetrical 27-level multilevel topology. The proposed inverter topology requires only 12 active switches instead of the 52 required in the conventional cascaded H-bridge [21]. In order to improve the conversion efficiency of conventional boost converters, a high step-up converter is introduced as a front-end stage to stabilize the output dc voltage of each DER modules for use with the simplified multilevel inverter. Finally a Twenty Seven-level output is observed by giving three supply voltages to the multilevel inverter. To develop the model of hybrid multilevel inverter, a simulation is done based on MATLAB/SIMULINK (version 7.12) is used.

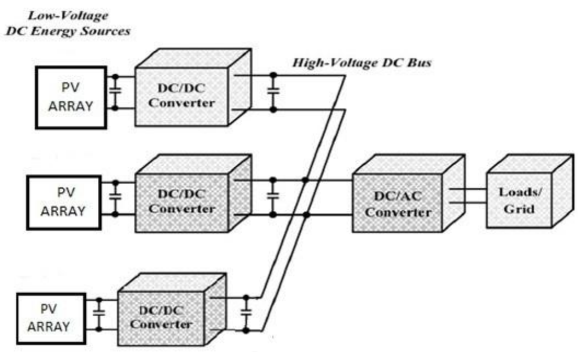

Figure 5: Configuration of DER Based Single-Phase Asymmetrical 27 Level Inverter Topology

VII. SIMULATIONS RESULTS

To verify the feasibility of the DER based single-phase asymmetrical 27-level inverter, a widely used software program MATLAB-Simulink is applied to simulate the circuit according to the previously mentioned operation principle. Input sources, the output voltages of each pv array are 30v, 90v,270v respectively are connected is as shown in fig 6 to the inverter followed a linear resistive load through the high step-up dc/dc converters. High step-up converter topology in used to boost and stabilize the output dc voltage of DER such as various PV arrays for employment of the proposed simplified multilevel inverter The three input voltage sources feeding from the high step-up converter is controlled at V_{dc1} = 100v, $Vdc2 = 3\ V_{dc1}$, $Vdc3 = 9\ V_{dc1}$.The proposed prototype of 27 level inverter is shown in fig 7 and corresponding lower inverter generates a fundamental output voltage of 1280V using three individual DC sources. The harmonic spectrum is as shown fig 9. Based on the simulation results, the proposed multilevel inverter was tested by a prototype. Components comparison between conventional inverters and the proposed approach appearing 27 output levels is given in Table 2. It is compared with the conventional multilevel inverters, i.e., diode-clamped, flying capacitor, cascaded H-bridge, and cascaded transformer based multilevel inverter. In the case of diode-clamped, a large number of clamping diodes are a severe drawback. And a lot of balancing capacitors is a disadvantage of the flying capacitor method. Among them, the isolated CML looks very effective to synthesize output voltage levels. It only needs a single dc input source. However, it shows low. Efficiency because of adopting a cascaded transformer. And it will be suffered from large size and heavy weight. Moreover, this method is not desirable for the motor drives employing VF (variable frequency) control scheme because of the saturation of transformer.

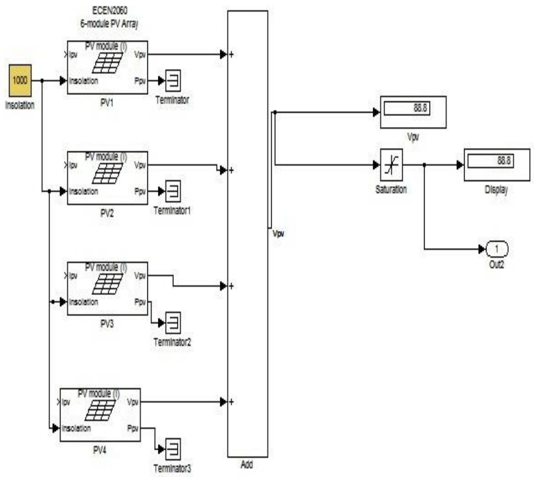

Figure 6: Simulation of Pv Array

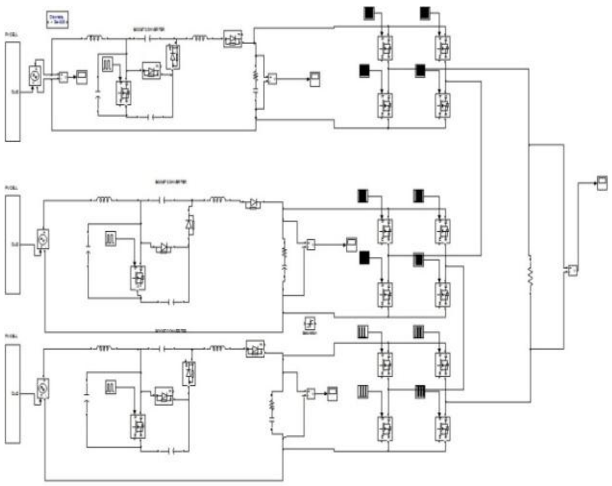

Figure 7: Simulation of Main Circuit

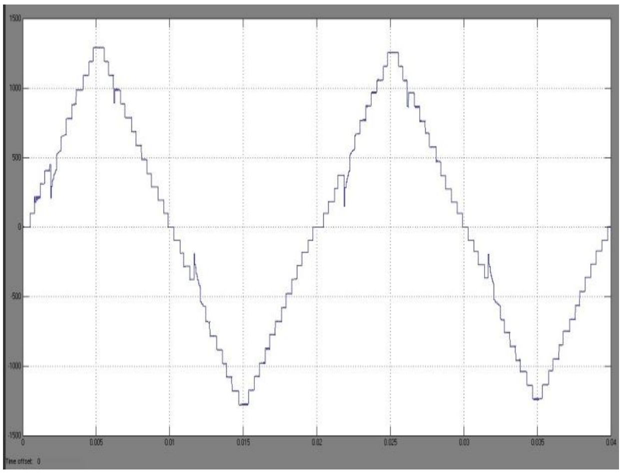

Figure 8: Twenty Seven level output

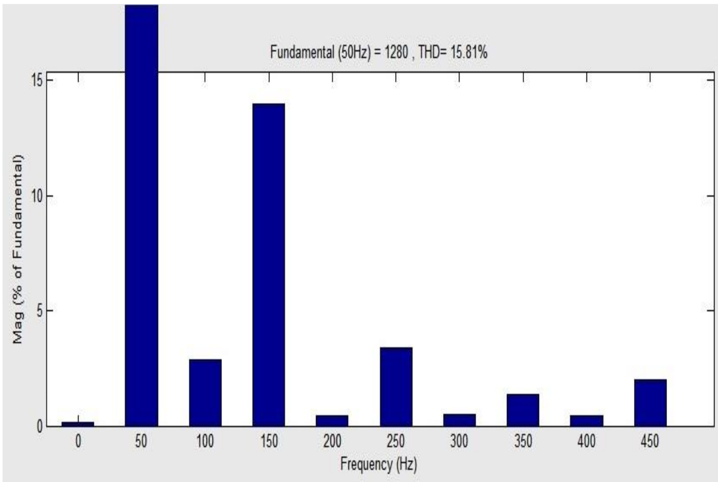

Figure 9: FFT Analysis of Twenty Seven level output

	Cascade	Hybrid	Proposed Prototype
No of level S = 3	2S+1, 7 level	$2^{S+1} - 1$, 15 level	3^{s},27 level
Input DC Voltage	V_{dc} , 1 V_{dc}	$2^{S-1}\ V_{dc}$, 4 V_{dc}	$3^{S-1}\ V_{dc}$, 9 V_{dc}

Table.2 Comparison of different Topologies

From the comparison, it is clear that the most outstanding advantage of the proposed multilevel inverter scheme is the elimination of transformer in the main power stage. However, each cell of the proposed multilevel inverter requires its own isolated power supply. The provision of these isolated supplies is the main limitation in the power electronic circuit design. So the proposed multilevel inverter is suitable for photovoltaic power generating systems equipped with distributed power sources.

VIII. CONCLUSION

In this Paper much effort has been focused on the development of environmentally friendly distributed energy resources (DERs) along with cascaded H-bridge multilevel inverter employing trinary dc sources to obtain a large number of output voltage levels with minimum devices.

The proposed inverter can synthesize high quality output voltage near to sinusoidal waves. The circuit configuration is simple and easy to control. The proposed prototype consists of three dc sources with the use of 12 switches Valuable and presentable merits of the proposed approach are summarized as

(1) Economical circuit configuration to produce multilevel outputs by using trinary input sources,
(2) Easy to increase of the output voltage levels and output power owing to modularity characteristic,
(3) Little transition loss of switches due to low switching frequency and reduced EMI; it is suitable for high voltage applications.

instead of 52 switches for conventional H bridge inverter to get required 27 level output voltage. The operational principle and key waveforms are illustrated and analyzed.

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