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A New Phase Shifted Converter using Soft Switching Feature for Low Power Applications

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Abstract: *This project presents a new dual bridge DC/DC converter for Low power applications which can solve the drawbacks of conventionally existing phase-shifted full bridge converters. It eliminates the narrow zero voltage switching (ZVS) range. The proposed converter configuration is composed of leading leg and lagging leg SHBIs. Phase shift control is employed to control the phase difference between the two bridge inverters. By shifting the phase, the converter changes the two inverters output voltage overlapping area to regulate its output voltage. At the secondary side, a centre tapped rectifier with two low current ratings are used. This structure allows the proposed converter to have the advantages of full ZVS range. ZVS eliminates turn on switching loss of the power switch. In this paper, the circuit analysis, operating principle and relevant analysis results of the proposed converters are presented.*
Index terms: *Full bridge converter, phase shift control, zero voltage switching.*

I. Introduction

DC voltage power supplies are utilized in most electrical/electronic equipment in order to meet the power requirement of the electronic circuits in the equipment. At higher power, voltage, or current ratings more complex power converters become necessary. When galvanic isolation or a significant voltage/current level change is required, these converters are accompanied with an isolation transformer. However, the converter suffers from an increased loss in the duty cycle, and a severe reverse-recovery phenomenon is generated on the additional clamping diodes when there is a light load [1], [2]. , In addition, the small duty cycle has detrimental effects on converter performance, such as a large ripple current through the output inductor LO [3]and the ZVS range of lagging-leg switches is very narrow under load variation. For this reason, its conversion efficiency is severely degraded as the load decreases [4].PSFB converters extending the ZVS range without the increase of duty-cycle loss were introduced in [6]–[9]. In the converters, however, the current stress of all the switches is higher than the traditional PSFB converter due to the assistant current source for a wide ZVS range, which leads to the increase in conduction loss. To minimize the increase of current stress, one or two bulky inductors and some coupled inductors with large inductance are additionally required. The PSFB converters with a current-doubler rectifier can also solve the problems. However, the current ripple of two output inductors must be designed to be very large for a wide ZVS range. This results in an increase of RMS current stress in the converters [10], [11]. In [12] and [13], the PSFB converters with two transformers were introduced. Due to the use of two transformers, the ZVS operation in the converters is achieved under entire load conditions. However, the dc bias currents equal to half the primary-reflected load current, which flows through the transformers, reduce the utilization of the transformers. The PSFB converters with ZVS and zero-current-switching (ZCS) operation can provide another solution to the problems. In these converters, leading-leg switches are turned ON with ZVS and lagging-leg switches are turned OFF with ZCS. Thus, MOSFETs as leading-leg switches and IGBTs as lagging-leg switches are generally employed. Because the ZVS operation of leading-leg switches is achieved by the same way as that of the traditional PSFB converter, its range is wide under load variation. Moreover, nearly constant efficiency can be obtained over a wide input voltage range because there is no circulating current in the converters. However, for ZCS operation and countermeasures to side effects such as high secondary-voltage stress and primary-current overshoot, they require many additional components, which results in high cost and a complex structure [14]–[17]. In addition, using IGBTs to suit ZCS operation precludes the use of high switching frequency to realize smaller magnetic components and capacitors [18]–[19].

The objective is to develop a soft switching converter that achieves zero voltage switching over a widely varying load for low power applications. In this paper a new soft-switching dc/dc converter with a full ZVS range for high voltage applications is developed. It is composed of two symmetric half bridge inverters (leading leg and lagging leg SHBIs, which are placed in parallel on the primary side and are driven in a phase shifting manner to regulate the output voltage. This structure allows that the proposed converter has

the following advantages that All the switches is turned ON with ZVS under entire load conditions without any additional large resonant inductors or circuits, while the conduction loss caused by the assistant current source extending the ZVS range is minimized due to its reduced conduction path.

II. Proposed Converter Configuration

In order to overcome the problems of the traditional PSFB converter, many studies have been conducted. First, to remove the circulating current and reduce the large output inductor, the frequency modulated FB converter was developed. The operating range of its switching frequency, however, is very widely changed in a wide input voltage range, which leads that it is difficult to design optimally the magnetic components and capacitors. In addition, the converter cannot achieve ZVS in a wide range of load variation. The ZVS range of lagging leg switches in the traditional PSFB converter can be extended by making the leakage inductance of the transformer very large and/or adding an external resonant inductor with large inductance. However, this approach increases duty cycle loss, which results in high secondary voltage stress and primary conduction losses. Another PSFB converter uses a resonant inductor to extend the ZVS range of lagging leg switches and needs two clamping diodes for easy reduction of the secondary voltage overshoot and oscillation, However converter suffers from increased duty cycle loss.

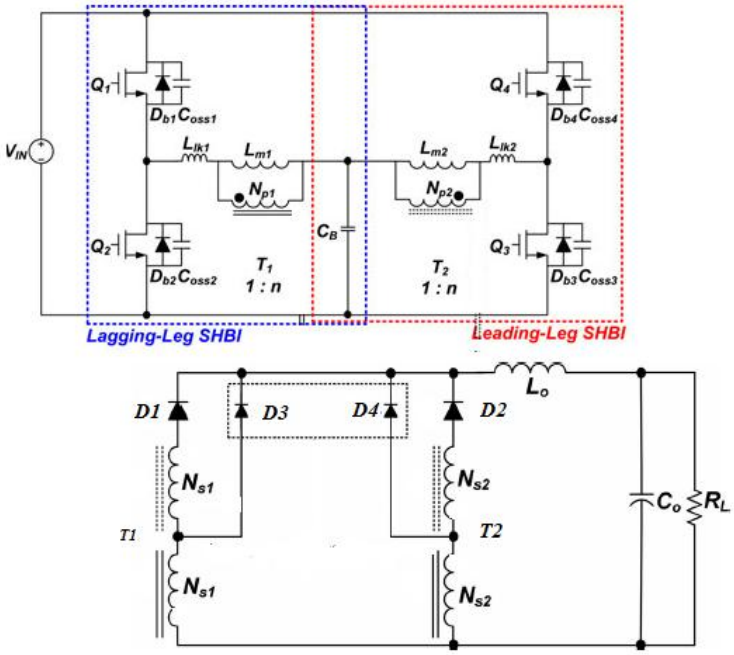

Fig.2.Proposed converter

The proposed system presents a new soft switching dc/dc converter with a full ZVS range for medium voltage applications is proposed. The proposed converter is composed of two symmetric half bridge inverters (TSHBIs), leading leg and lagging leg SHBIs, which are placed in parallel on the primary side and are driven in a phase-shifting manner to regulate the output voltage

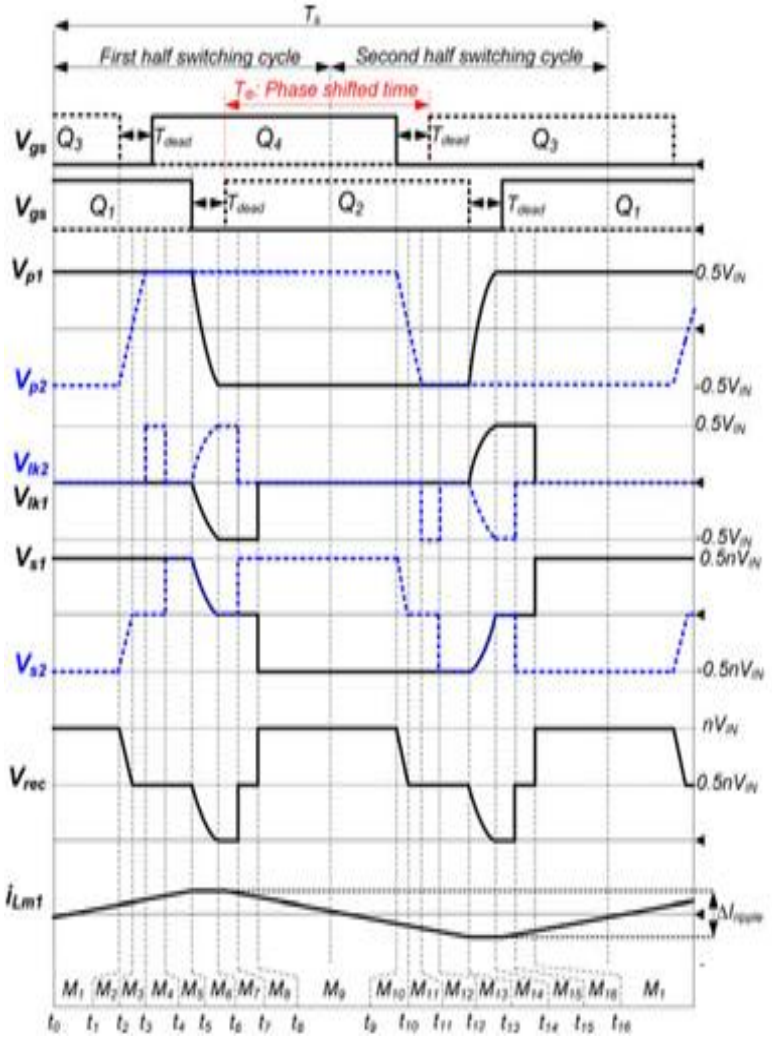

Fig.3.Operating waveforms

III. Principle of Operation

The circuit diagram of the proposed converter is shown in Fig.2. The primary side consists of four switches and two transformers transferring the input power to the secondary side alternately. Fig. 3 shows the operating waveforms of the proposed converter in the steady state,

Mode 1[t_0-t_1]: Mode 1 begins when switches Q_1 and Q_3 are in on-state and diodes D_1 and D_3 are conducting. During this mode, the primary voltages $V_{p1}(t)$ and $V_{p2}(t)$ of the transformers T_1 and T_2 are the positive and negative halves of the input voltage, respectively. Thus, the magnetizing current $\mathbf{i}_{Lm1}(t)$ increases linearly from its initial value. However, $\mathbf{i}_{Lm\ 2}(t)$ is nearly zero because the magnetizing inductance L_{m2} of T_2 is very large. The secondary voltages $V_{s1}(t)$ and $V_{s2}(t)$ of T_1 and T_2 are the positive and negative halves of the input voltage reflected to the secondary by the turns ratio n, respectively, thus the power is transferred from the input to the output through T_1, T_2, D_1, and D_3. The output voltage of rectifier $V_{rec}(t)$ becomes nV_{IN}, which is the sum of $V_{s1}(t)$ and $-V_{s2}(t)$. The primary currents in this mode can be expressed as follows:

$i_{p1}(t) = i_{Lm1}(t) + ni_{sec1}(t) = i_{Lm1}(t) + ni_{D1}(t)$

$= i_{Lm1}(t) + nI_o$

$i_{p1}(t) = i_{Lm2}(t) + ni_{sec2}(t) \approx ni_{sec2}(t) = - ni_{D3}(t) = -nI_0$ (1)

Mode 2[t_1-t_2]: Mode 2 begins when Q_3 is turned OFF at t_1. Then, the voltage across C_{oss3} is charged linearly and the voltage across C_{oss4} is discharged linearly by the energy stored in the output inductor L_o .$V_{p2}(t)$ increases from $-0.5V_{IN}$ to zero and $V_{p1}(t)$ is continuously maintained at $0.5V_{IN}$, which

increases continuously $\mathbf{i}_{Lm1}(t)$.$V_{s2}(t)$ also increases from $-0.5nV_{IN}$ to zero and $V_{s1}(t)$ becomes $0.5nV_{IN}$. Thus, $V_{rec}(t)$ falls from nV_{IN} to $0.5nV_{IN}$. The expressions of primary currents in this mode are the same as in mode 1. The voltages can be expressed as follows:

$$V_{Q3}(t) = \frac{nI_o}{2Coss}(t-t_1),\ V_{Q4}(t) = V_{IN} - V_{Q3}(t)$$

$$V_{p2}(t) = -0.5V_{IN} + \frac{nI_0}{2C_{oss}}(t-t_1)$$

$$V_{rec}(t) = V_{s1}(t) + V_{s2}(t) = nV_{IN} - \frac{n^2I_o}{2C_{oss}}(t-t_1) \qquad (2)$$

Mode 3[t_2-t_3]: Mode 3 begins when $V_{p2}(t)$ becomes zero in mode 2. At the same time, $V_{s2}(t)$ becomes zero and the voltage across C_{oss3} or C_{oss4} is continuously charged or discharged by the resonance, respectively. $V_{p2}(t)$ increases from zero to $0.5V_{IN}$ with a sinusoidal waveform and $V_{p1}(t)$ is continuously maintained at $0.5V_{IN}$. The voltages and currents in this mode are given by

$$V_{p1}(t) = 0.5V_{IN},\ V_{s1}(t)=0.5nV_{IN},V_{s2}(t)=0$$

$$V_{rec}(t) = 0.5nV_{IN},V_{p2}(t)=nI_{ozo1}\sin\omega_{o1}(t-t_2)$$
$$V_{Q3}(t) = 0.5V_{IN} +nI_{ozo1}\sin\omega_{o1}(t-t_2)$$
$$V_{Q4}(t) = V_{IN}-V_{Q3}(t),\ i_{p1}(t) = i_{p2}(t_2)+ \frac{0.5V_{IN}(t-t_2)}{L_{m1}}$$
$$i_{p2}(t) = -nI_o\cos\omega_{o1}(t-t_2)$$

where

$$\omega_{o1}= \frac{1}{\sqrt{2L_{lk2}C_{oss}}} \qquad z_{o1}= \sqrt{\frac{L_{lk2}}{2C_{oss}}} \qquad (3)$$

Mode 4[t_3-t_4]: Mode 4 begins when $V_{p2}(t)$ reaches $0.5V_{IN}$ in mode 3. Then, the parasitic diode D_{b4} of Q_4 starts to conduct and Q_4 is turned ON with ZVS. During this mode, $V_{s2}(t)$ is maintained at zero, thus the voltage $0.5V_{IN}$ appears on the leakage inductor L_{lk2}. Due to this voltage across L_{lk2}, the commutation of D_3 is progressed .$V_{p1}(t)$ and $V_{rec}(t)$ are continuously maintained at $0.5V_{IN}$ and $0.5nV_{IN}$, respectively. During this mode, the power is transferred from the input to the output through T_1, T_2, D_1 and D_3. The currents in this mode can be expressed as follows:

$$i_{p1}(t) = i_{p1}(t_3) + \frac{0.5V_{IN}(t-t_3)}{L_{m1}}$$
$$i_{p2}(t) = -nI_o + \frac{0.5V_{IN}(t-t_3)}{L_{lk2}},\quad i_{D1}(t) =Io$$
$$i_{D3}(t) = Io \qquad (4)$$

Mode 5[t_4-t_5]: Mode 5 begins when the commutation of D_3 is completed at t_4 and only D_1 conducts. In this mode, the primary current $\mathbf{i}_{p2}(t)$ [or the secondary current $\mathbf{i}_{sec2}(t)$] in leading-leg SHBI is zero, i.e., the power is transferred from the input to the output through only T_1 and D_1,. During this mode, the voltages and currents are given by

$$V_{p1}(t) = V_{p2}(t) = 0.5V_{IN} ,\ V_{s1}(t) = V_{s2}(t) =0.5nV_{IN},$$
$$V_{rec}(t) = 0.5\ nV_{IN} ,i_{p1}(t) = i_{p1}(t_4)+ \frac{0.5V_{IN}(t-t_4)}{L_{m1}}$$
$$i_{p2}(t) = ni_{sec2}(t) = 0 \qquad (5)$$

Mode 6[t_5-t_6]: Mode 6 begins when Q_1 is turned OFF at t_5. At the same time, diode D_4 starts to conduct. Then, the resonance of C_{oss1}, C_{oss2}, L_{lk1}, and L_{lk2} occurs in the primary power path. The voltage across C_{oss1} or C_{oss2} is discharged or charged by the resonance, respectively. $V_{p1}(t)$ is decreased from $0.5V_{IN}$ to $-0.5nV_{IN}$ and $V_{rec}(t)$ falls to zero. The commutation between D_1 and D_4 is also progressed. The voltages and currents in this mode can be expressed as follows:

$$V_{Q1}(t) = V_{IN} - V_{Q2}(t)$$
$$V_{Q2}(t) = V_{IN} - z_{o2}\mathbf{i}_{p1}(t_5)\sin\omega_{02}(t-t_5)$$
$$V_{p1}(t) = 0.5V_{IN} - z_{o2}\mathbf{i}_{p1}(t_5)\sin\omega_{o2}(t-t_5)$$
$$V_{p2}(t) = 0.5V_{IN}$$
$$V_{s1}(t) = V_{s2}(t) = V_{rec}(t)$$

$$= 0.5nV_{IN} - n\omega_{o2}L_{lk2}\mathbf{i}_{p1}(t_5)\sin\omega_{o2}(t-t_5)$$
$$\mathbf{i}_{p1}(t) = \mathbf{i}_{p1}(t_5)\cos\omega_{o2}(t-t_5)$$
$$\mathbf{i}_{p2}(t) = (n\mathbf{I}_o+0.5\Delta\mathbf{I}_{ripple}) - \mathbf{i}_{p1}(t_5)\cos\omega_{o2}(t-t_5)$$
$$i_{D4}(t) = I_o - i_{D1}(t) = i_{p2}(t)/n$$

where

$$i_{p1}(t_5) = nI_o = 0.5\Delta I_{ripple},\ \Delta I_{ripple} = \frac{V_{IN}Ts}{4L_{m1}}$$

$$\omega_{o2} = \frac{1}{\sqrt{2(L_{lk1}+L_{lk2})C_{oss}}},\ z_{o2} = \sqrt{\frac{L_{lk1}+L_{lk2}}{2C_{oss}}} \qquad (6)$$

Mode 7[t_6-t_7]: Mode 7 begins when $V_{p1}(t)$ reaches $-0.5V_{IN}$ in mode 6. Then, the parasitic diode D_{b2} of Q_2 starts to conduct and Q_2 is turned ON with ZVS. In this mode, all the secondary voltages of the transformers, $V_{sec1}(t)$ and $V_{sec2}(t)$, are zero, thus $V_{rec}(t)$ becomes zero. Due to $V_{rec}(t)$=0, the load power is supplied from the energy stored in the output inductor L_o at t_6.Because $V_{p1}(t)$=-0.5V_{IN}, $V_{p2}(t)$=0.5V_{IN}, and $V_{s1}(t) = V_{s2}(t) = 0$ during this mode, the voltage $V_{lk1}(t)$ across L_{lk1} equals to $-0.5V_{IN}$ and the voltage $V_{lk2}(t)$ across L_{lk2} equals to 0.5V_{IN}. Due to these leakage inductors' voltages, $\mathbf{i}_{p1}(t)$ or $\mathbf{i}_{D1}(t)$ decreases linearly and $\mathbf{i}_{p2}(t)$ or $\mathbf{i}_{D4}(t)$ increases linearly. The currents can be expressed as follows:

$$i_{p1}(t) = i_{p1}(t_6) - \frac{0.5V_{IN}(t-t_6)}{L_{lk1}}$$
$$i_{p2}(t) = i_{p2}(t_6) + \frac{0.5V_{IN}(t-t_6)}{L_{lk2}}$$
$$i_{D4}(t) = I_o - i_{D1}(t) = i_{p2}(t)/n \qquad (7)$$

Mode 8[t_7-t_8]: Mode 8 begins when the current through D_4, $\mathbf{i}_{D4}(t)$, reaches the output current $\mathbf{I}_o$ and D_1 is naturally turned OFF. At the same time, $V_{s1}(t)$ becomes zero and $V_{s2}(t)$ becomes 0.5nV_{IN}. Thus, during this mode, the voltage 0.5V_{IN} appears on L_{lk1}, and the commutation of D_2 starts. $V_{rec}(t)$ equals to 0.5nV_{IN}. The currents in this mode can be expressed as follows:

$$i_{p1}(t) = i_{p1}(t_7) - \frac{0.5V_{IN}(t-t_7)}{L_{lk1}},\ i_{p2}(t) = nI_o$$
$$i_{D4}(t) = I_o,\ i_{D2}(t) = I_o - \frac{0.5V_{IN}(t-t_7)}{nL_{lk1}} \qquad (8)$$

At the end of this mode, $\mathbf{i}_{D2}(t)$ reaches the output current $\mathbf{I}_o$. Then, the power is transferred from the input to the output through T_1, T_2, D_2, and D_4.

Mode 9-16[t_8-t_{16}]: The operations from mode 9 to mode 16 are the same as previous modes except for the direction of powering path.

IV. Experimental Results

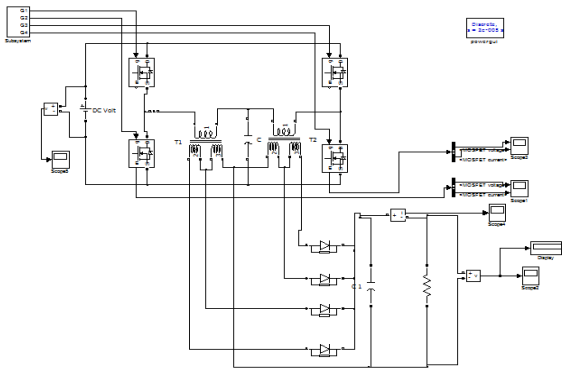

Fig.4.Simulation Circuit

Digital simulation is done using MATLAB and the results are presented here. Open loop system of 200V/48V, 100 KHz dc/dc converter is shown in Fig.4.Input voltage of 200V is shown in

Fig.5. The output voltage in open loop system is shown in Fig.8.. The output current is shown in fig.9. The output voltage increases with the increase in the input voltage. Figs.6. and 7 shows the ZVS waveforms of the leading-leg or lagging-leg SHBIs. From Figs. 6 and 7, it is clear that all the switches in the proposed converter are turned ON with ZVS under entire load conditions.

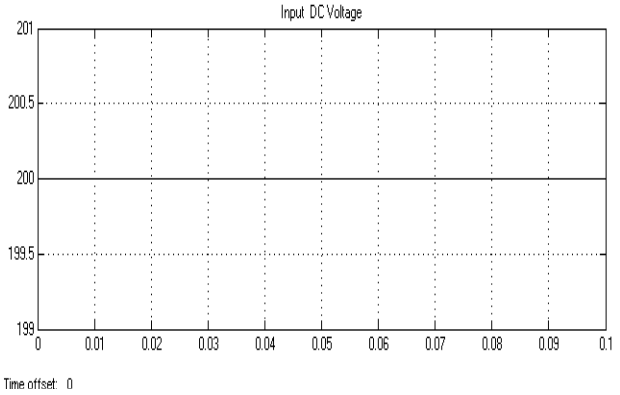

Fig.5.Input DC voltage

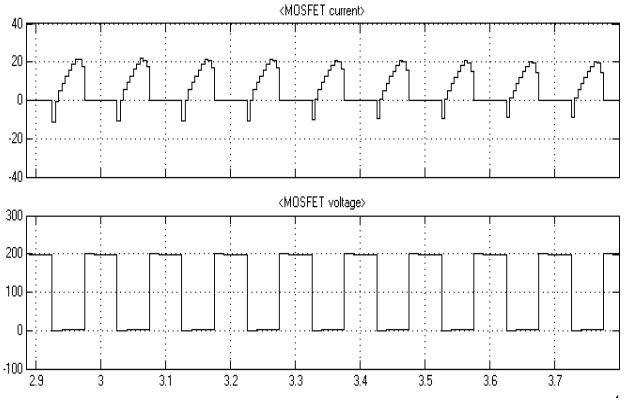

Fig.6.Waveform indicating ZVS condition of the lagging-leg switch Q_2

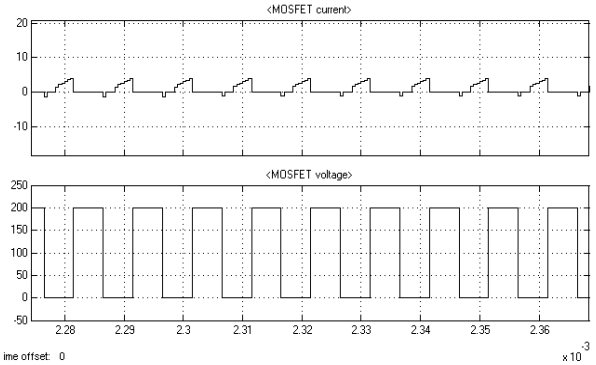

Fig.7.Waveform indicating ZVS condition of the leading-leg switch Q_3

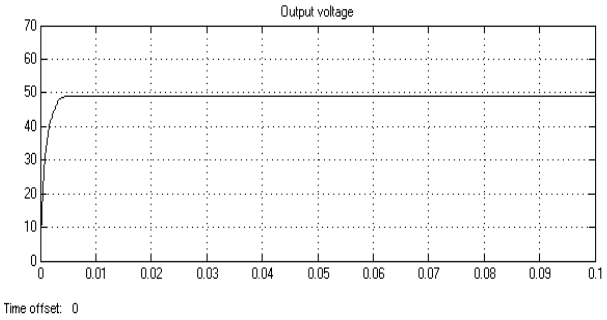

Fig.8.Converter output voltage

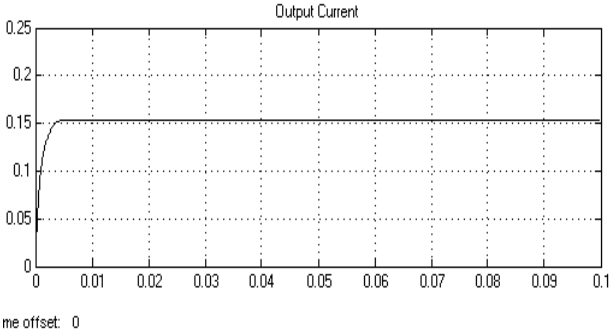

Fig.9.Converter output current

VI. Conclusion

In this paper a new soft-switching dc/dc converter with a full ZVS range for low voltage applications is developed. It is composed of two symmetric half bridge inverters (leading leg and lagging leg SHBIs, which are placed in parallel on the primary side and are driven in a phase shifting manner to regulate the output voltage. With an auxiliary centre tapped rectifier at the secondary side with two low current rating diodes, Zero voltage switching of the switches are achieved. This DC/DC converter is relatively suitable for low power applications. Moreover, the proposed converter can be integrated with other to achieve soft-switching feature. A prototype has been designed to prove the validity of the proposed converter. The proposed converter is suitable for the server and telecommunication equipments using 48 V bus voltage, and requiring the high efficiency and high power density. Also, in the near future, it is suitable for the new automotive 48 V power systems.

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