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Performance Improvement of Delta Sigma Modulator for Wide-Band Continuous-Time Applications

Parvathy Unnikrishnan[1], Siva Kumari C.[2], Jayakrishnan K.R.[3]
[1,2] *PG Scholar, VLSI & Embedded Systems, College of Engineering Munnar, India*
[3] *Assistant Professor, Dept. of Electronics & Communication, College of Engineering Munnar, India*

ABSTRACT:- *Data converters are the key components in any electronic system, as they allow the flow of signals between analog and digital world. Recently, Delta Sigma Modulators (DSM) especially Continuous-time DSM (CT-DSM) have started attracting interest in wireless applications for their low power consumption and wider input bandwidth. Unlike conventional converters, DSM has two main features, Oversampling and Noise shaping. Oversampling feature eliminates the need for abrupt cut-offs in anti-aliasing filter. Noise-shaping shapes the quantization noise out of the band-of-interest. In this paper a Wide-band CT-DSM is designed in a standard 180nm technology in Cadence Virtuoso tool. A two stage op-amp is first designed and implemented, which is used for implementing rest of the blocks of DSM such as the Summing amplifier, Comparator and an Integrator. In addition to these blocks, a Digital-to-analog converter (DAC) is also implemented, as a feedback loop.*

Keywords: *Continuous-time, Delta Sigma Modulator, Noise shaping, Op-amp, Oversampling*

I. INTRODUCTION

The major innovations that are taking place in the present scenario require large data rate, high resolution and low power. As the conventional converters cannot satisfy these requirements there was a need for the development of a data converter that can satisfy these requirements. Thus, Delta Sigma Modulator (DSM) became one of the most popular data converters in mixed signal VLSI process, as they satisfy the needs of present day technology developments.The Delta-Sigma Modulators have been in existence for many years, the recent technological advances made the device practical and their use is becoming widespread. Continuous-time DSM provides high resolution and dynamic range and hence they are used in high speed wireless applications. The main objective of this research is to design a Wide-band Continuous-time Delta-Sigma modulator (CT-DSM) in CMOS technology.

I. 1 BIT FIRST ORDER DELTA SIGMA MODULATOR

The name Delta Sigma Modulator was introduced by Inose in 1962 in his paper discussing about 1-bit converters. In the 70s, because of the initially limited performance of Delta Sigma Modulators, their main use was in encoding low frequency audio signals (analog-to-digital conversion) using a 1-bit quantizer and a first[2] or a second order loop filter. Delta-sigma converters are ideal for converting signals over a wide range of frequencies from dc to several megahertz with very-high-resolution results. Unlike conventional data converters, which uses Nyquist rate (fs>2fm) for sampling, DSM uses Oversampling (fs>>2fm) for sampling the input signal. When the signal is oversampled, the quantization noise spreads over a wider bandwidth, the total quantization noise remaining still the same, but the noise at the band of interest is reduced considerably.

The Delta-sigma modulator comes under Oversampling data converters, since they use Oversampling technique. The use of Oversampling Delta-sigma modulators in the integration of high-resolution analog-to-digital converters has shown promise for overcoming the analog component limitations inherent in modern VLSI technologies. Increasing the sampling rate relaxes the need for using anti-aliasing filters. By sampling at a frequency that is much greater than the signal bandwidth, t is possible for the feedback loops to shape the quantization noise so that most of the noise power is shifted out of the signal band a process called Noise shaping.

The process of noise shaping by the DSM can be viewed as pushing quantization noise power from the signal band to higher frequencies. The out-of -band noise can then be attenuated with a digital filter. The degree

to which the quantization noise can be attenuated depends on the order of the noise shaping and the oversampling ratio.

CT-DSM consists of a Summing amplifier, Loop filter, an Analog-to-digital (ADC) converter and a Digital-to-analog converter (DAC) as a feedback loop. The analog input is given to the inverting terminal of the Summing amplifier and the non-inverting terminal is grounded. The output of the Summing amplifier is connected to an Integrator which is the loop filter. The integrated output is given to the input of a Comparator. The Comparator used here works as a 1-bit ADC. Its output is connected to a DAC. The DAC output is connected to the Summing amplifier. The difference between the analog input and the DAC output is taken. This process is continuous in the closed loop.

II. BASIC BUILDING BLOCKS OF DSM

The CT-DSM consists of Summing amplifier, an Integrator, Comparator, feedback DAC [5]. The Summing amplifier, Integrator and the Comparator is designed using a two stage op-amp. Fig 3.1 shows the block diagram of a First order Delta Sigma Modulator.

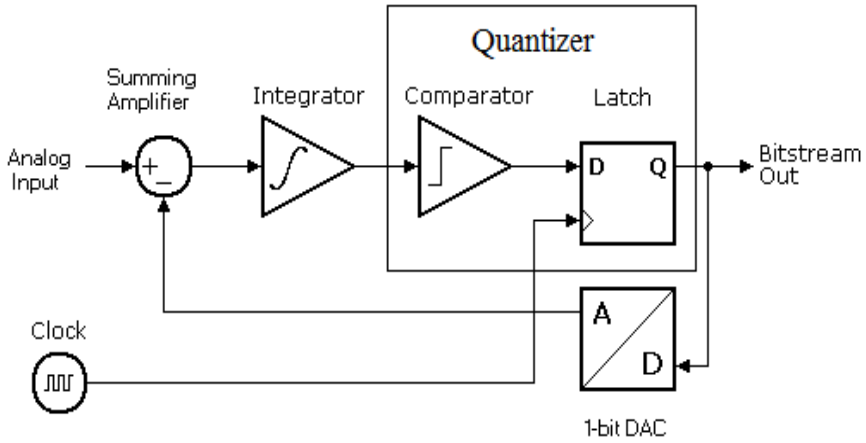

Fig 1: Block diagram of DSM

The Summing amplifier is the first block of a CT-DSM. It is designed using the two stage op-amp. The analog input and the feedback output signal from DAC is given to the inverting terminal of the Summing amplifier. The non-inverting terminal is connected to ground. The output of the Summing amplifier is given to the input of the next block which is the Integrator.
The Integrator acts as the Loop filter. This circuit shapes the noise out of signal bandwidth. A simple RC integrator will do this property. The RC Integrator is an operational amplifier circuit which performs the mathematical operation of integration.

The Quantizer consists of a Comparator and a D latch. The Comparator is designed using the op-amp. Basically Comparator is a 1-bit analog to digital converter. The main function of the Comparator is to compare the applied input signal voltage with the reference voltage and generate an output digital signal, based on the comparison. The output of the Comparator is given to the input of D latch. The D latch is used to provide the Oversampling concept. It is implemented using transmission gates and cascading two inverter circuits. When CLK goes high, D is transmitted to output Q and when CLK goes low, the latch retains its previous state. The clock frequency determines the Oversampling ratio.

The feedback loop of a CT-DSM has a Digital-to- analog converter. It is a device for converting a digital usually binary code to analog signal (current, voltage or charges). The designed CT-DSM is first order and to analyze the loop delay a particular delay element is needed, to provide the delay two inverters are cascaded together.

Continuous-time DSM is designed by cascading the Summing amplifier, Integrator, Quantizer and the DAC, in the feedback path. The op-amp is the core part to design the Summing amplifier, Integrator and Comparator.

III. DESIGN OF DSM

The designing of different blocks and the Continuous-time DSM is designed in 180nm Cadence Virtuoso tool. Operational amplifier is the core part of the CT-DSM. In this project a Wide-band two stage op-amp is designed inorder to implement the blocks of DSM. So a first stage op-amp was initially designed. Using this, the two stage op-amp was designed. The forward loop consisting of the Summing amplifier, Integrator and the Comparator, was implemented using this two stage op-amp. The Comparator along with a D latch form the Quantizer. The DAC in the feedback path was implemented by cascading two inverters.

1.1 Design of Two stage Op-amp

Op-amp is the core part, which is used to implement the rest of the blocks of DSM, such as the Summing amplifier, Integrator and Comparator. A first stage op-amp was designed using which the two stage op-amp was implemented [9]. A common source amplifier is cascaded with the first stage op-amp to form the two stage op-amp.

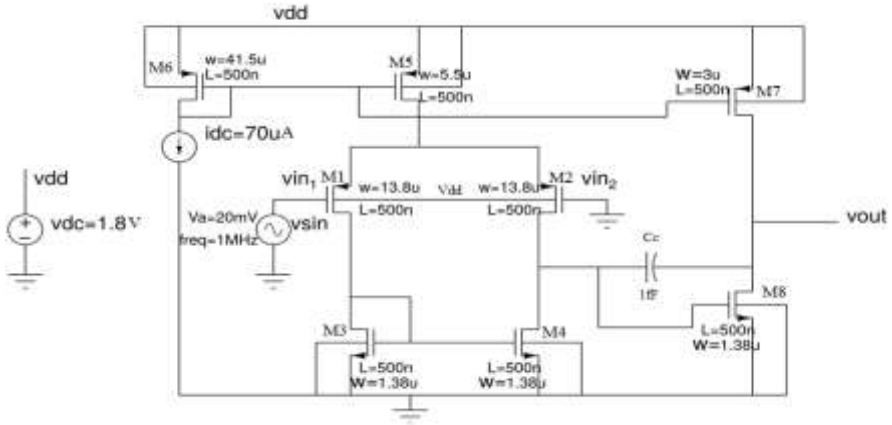

Fig 2: Schematic of two stage Op-amp

Table I: Design parameters of two stage Op-amp

Sl.No	Parameters	Design Specification	Output Specification
1	Technology	gpdk 180	gpdk 180
2	Supply voltage	1.8 V	1.8V
3	DC Gain	>=80dB	71.9dB
4	Unity Gain bandwidth	>=1GHz	800MHz
5	Phase margin	>60 degree	55 degree

The gain is around 71.9dB and the Unity Gain bandwidth is 800MHz.The phase margin obtained is about 55 degree.

1.2 Design of Summing amplifier

The Summing amplifier is the very first block of a CT-DSM flexible circuit based on the standard operational amplifier, which can be used for combining multiple inputs. It has a single input voltage applied to the inverting input terminal. The amplifier used in the summing amplifier is the same two stage Op-amp that was designed above.

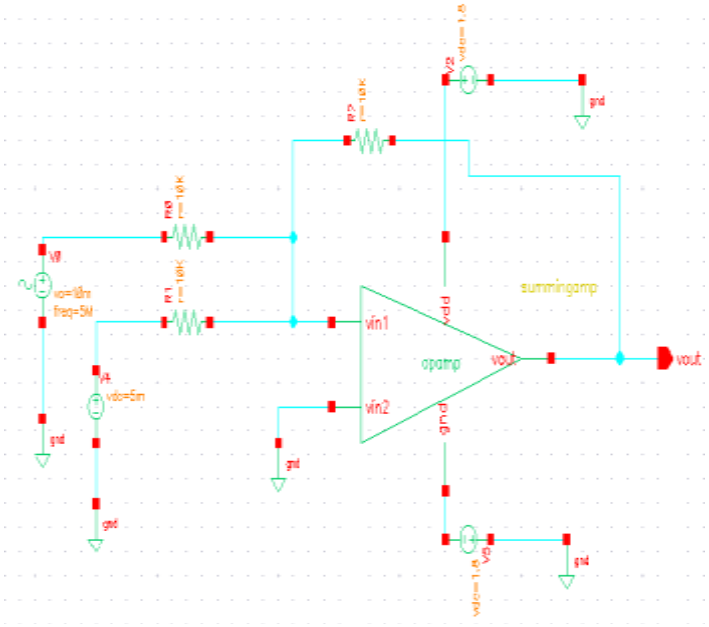

Fig 2: Schematic of Summing amplifier

1.3 Design of Integrator (Loop filter)

The RC Integrator is designed using the two stage op-amp with appropriate R and C values.

Cut-off frequency of Integrator, fo = 1/(2ΠCR3)

Choosing fo = 800MHz, R0 = 10KΩ and C = 1fF,

On substituting the values in the equation for fo,

R3 = 198.9KΩ. So taking R3 = 200KΩ.

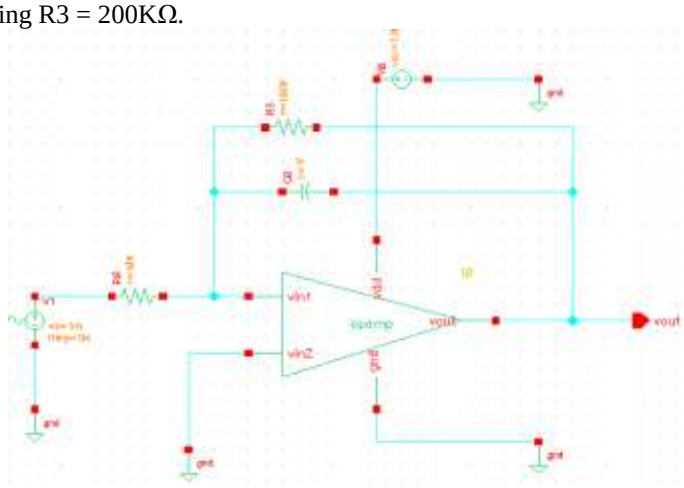

Fig 3: Schematic of Integrator

1.4 Design of Quantizer

The quantizer designed, has two parts; the first part is the Comparator and second is the D latch [10]. Comparator is designed using the op-amp. The D latch is implemented using transmission gates and inverters. The Quantizer is thus designed by cascading the Comparator and D latch.

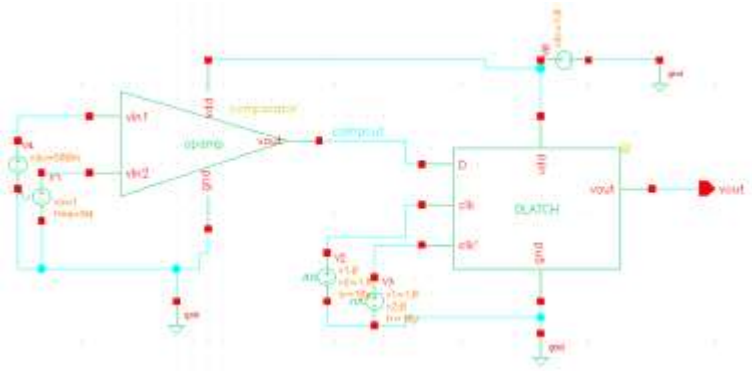

Fig 4: Schematic Of Quantizer

Analog input signal is given to the op-amp non-inverting terminal and reference signal is given to the inverting terminal. Hence the op-amp compares these two input signals and produces a digital output. Next section of the quantizer is the D-latch. The output of the comparator is given to the D input of latch. The D latch is used to provide the Oversampling concept.

1.5 Design of Digital-to-analog Converter (DAC)

The DAC comes in the feedback loop, where the output of DSM which is the same quantizer output itself is given as the feedback signal. The output of DAC is fed to the summing amplifier in the forward loop. In the single bit DSM the DAC has only two voltage levels either a high or a low. Hence the function of DAC is to convert these voltage levels to reference levels. In this case the reference levels are determined by maximum acceptable input DC levels of Summing amplifier. So we choose two cascaded inverters to design the DAC.

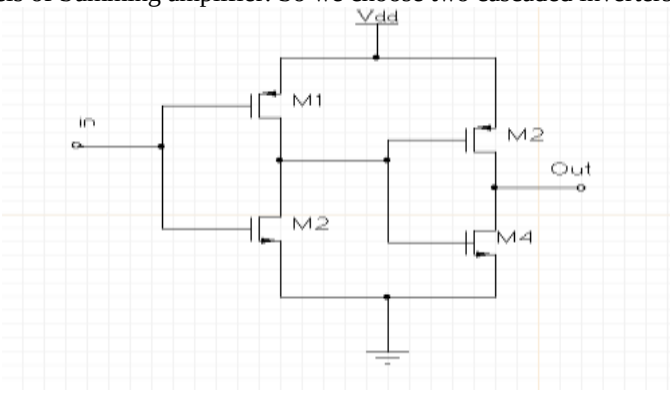

Fig 5: Schematic of DAC

1.6 Implementation of CT-DSM

The designed Summing amplifier, Integrator, Quantizer and DAC are combined to form the Continuous-time Delta-sigma modulator.

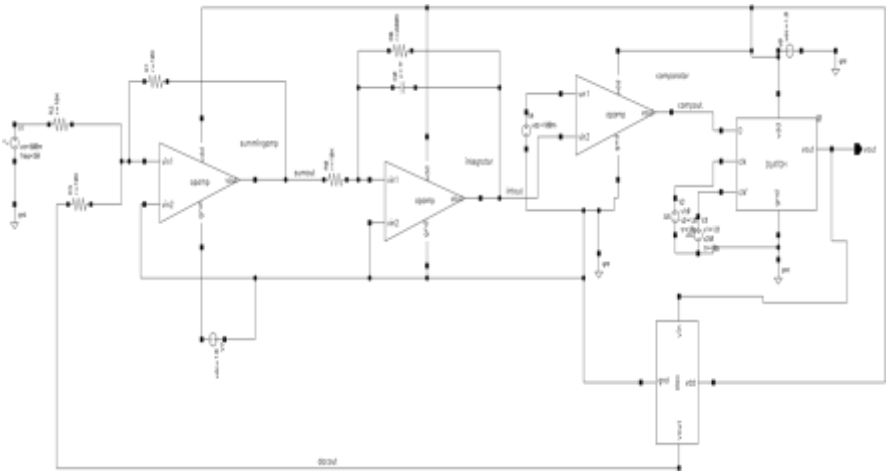

Fig 6: Schematic of CT-DSM

IV. SIMULATION RESULT

The Continuous-time DSM implemented is simulated in 180nm Cadence Virtuoso tool by combining all the major blocks such as the Summing amplifier, Integrator, Quantizer and DAC, which were separately designed and implemented. Fig 7 shows the final output transient response of the CT-DSM.

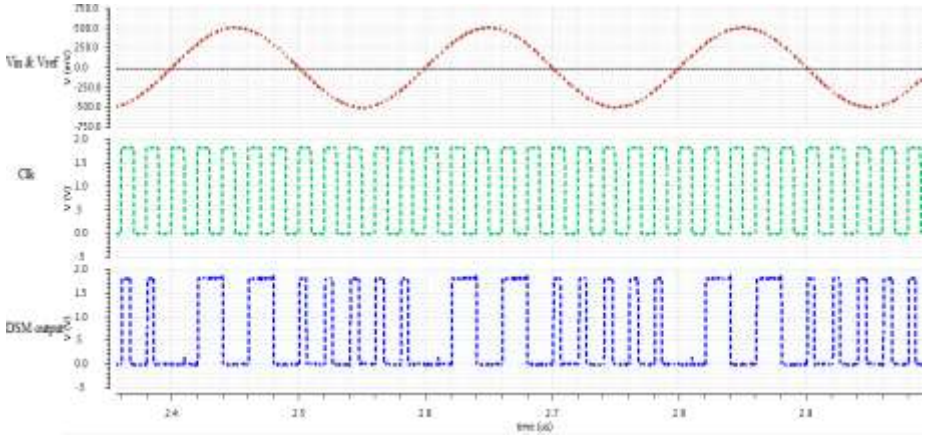

Fig 7: Output transient response of CT-DSM

V. CONCLUSION

The Continuous-time Delta-sigma modulators (CT-DSM) have been gaining more attention in recent years. Since the DSM have features such as Oversampling and Noise shaping, it can be used to achieve high resolution along with large bandwidth. A Wide-band Continuous-time DSM was designed. For this a wide band two stage op-amp was designed and implemented. Using this op-amp the major blocks of DSM such as Summing amplifier, Integrator and Comparator was implemented. Then inorder to form the Quantizer a D-latch was designed and combined with the Comparator. A DAC was implemented at the feedback path. Thus by combining all these blocks the CT-DSM was implemented in order to support the needs for requirements that are taking place in the current technology development.

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