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Total Harmonic Distortion Analysis and Comparison of Diode Clamped Multilevel Z-Source Inverter

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Abstract: *A desired AC voltage is achieved from several levels of DC voltages is done by multilevel inverters. These inverters are applied to high voltage and high power applications due to better harmonic spectrum and faithful output. In recent years a single X-shaped LC network is important development in multilevel inverters. The power quality improvement is obtained by reducing the harmonics present at the output voltage of the inverter. This paper presents the comparative THD analysis of several multicarrier PWM control techniques which is effectively used for harmonic mitigation in the proposed diode clamped multilevel Z-source inverter and this work is compared with conventional three level inverter by using MATLAB/SIMULINK.*

Keywords: *DCMLI, Multi-Carrier PWM control, Multilevel Inverter, Total Harmonic Distortion (THD), Z-Source Inverter.*

I. Introduction

In the recent years, the revolution of multilevel inverters has many attractive features. In particular, high voltage capability, reduced common mode voltages near sinusoidal outputs, lower value of dv/dt, smaller or even number output filters make multilevel inverter is a suitable topology for variable frequency induction motor drives and have recently been explored for low-voltage renewable grid interfacing applications [1]. Despite of their generally favourable output performance , NPC inverters are constrained by their ability to perform only voltage-buck operation if no additional dc–dc boost stages are added to their front-ends. To overcome this limitation, a buck–boost Z-source NPC inverter is proposed with reduced passive elements in [2]. Higher and lower carrier cells alternative phase opposition PWM technique was discussed for hybrid-clamped multilevel inverters [3]. Phase shift and phase opposition disposition PWM techniques were produces a same harmonic distortion in five level diode – clamped multilevel inverter, five level cascaded and hybrid inverters [4]. A zero harmonic distortion of the output wave can be obtained by an infinite number of levels. To synthesize multi level output ac voltage using different levels of dc inputs, semiconductors devices must be switched ON and OFF in such a way that desired fundamental is obtained with minimum harmonic distortion. There are different types of approaches for the selection of switching techniques for the multilevel inverters. The multilevel inverters are mainly controlled with sinusoidal PWM technique and the proposed inverter can reduce the harmonic contents by using multicarrier PWM technique arrangements [5]. Several types of PWM control techniques for various multilevel inverters are discussed [6], [7]. An additional X-shaped impedance networks are added between two isolated dc sources and a neutral clamped circuitry. The unique structure of the multilevel Z-source inverters allows them to reach high voltage with low harmonics without the use of transformers [8]. The various levels of NPC or DC inverters with space vector modulation are discussed in the references [9] - [11].

In proposed paper, various multicarrier PWM techniques like Phase disposition (PD), Phase opposition disposition (POD), Alternative phase opposition disposition (APOD), phase shifted (PS) are proposed for three phase five level diode clamped multilevel Z-Source inverter and the total harmonic distortion (THD) analysis is done for different modulation schemes. The proposed inverter can reduce the harmonic contents in the output phase voltages significantly. The total harmonic distortion (THD) reduction performance of three phases five level neutral clamped multilevel Z-Source inverter by using multicarrier PWM techniques are presented and the proposed work is compared with conventional three level diode clamped multilevel inverter.

II. Design And Operation of Diode Clamped Multilevel Inverter

The diode clamped inverter also known as neutral clamped inverter. The diode clamped inverter delivers the staircase output voltage using several levels of DC voltages developed by DC capacitors. If m is the number of level, then the number of capacitors required on the DC bus are (m-1), the number of power electronic switches per phase are 2(m-1) and the number of diodes per phase are 2(m-2). This design formula is most common for all the diode clamped multilevel inverters. The DC bus voltage is split into three levels using two capacitors C_1 and C_2, for five levels using four capacitors C_1, C_2, C_3 and C_4 are shown in Fig .1 and Fig .2. The voltage across each capacitor is $V_{dc}/4$ and the voltage stress across each switch is limited to one capacitor voltage through clamping diodes. The switching sequences of three phase 3-level and 5-level diode clamped multilevel inverter are shown in table. I and II. As the number of levels increase the harmonic distortion decreases and efficiency of the inverter increases because of the reduced switching losses. The number of levels in multilevel inverters is limited because of the large number of clamping diodes required. The reverse recovery of these diodes is especially with multicarrier PWM techniques in a high voltage application is a major design challenge.

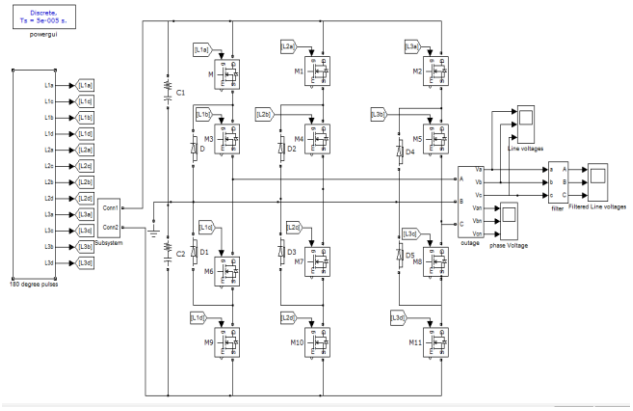

Fig.1.Three level diode clamped multilevel inverter

TABLE I
Three-level switching sequences

Terminal voltages	Switching sequences			
	S_{a1}	S_{a2}	S_{a3}	S_{a4}
$+v_{dc}$	On	On	Off	Off
0	Off	On	On	Off
$-v_{dc}$	Off	Off	On	On

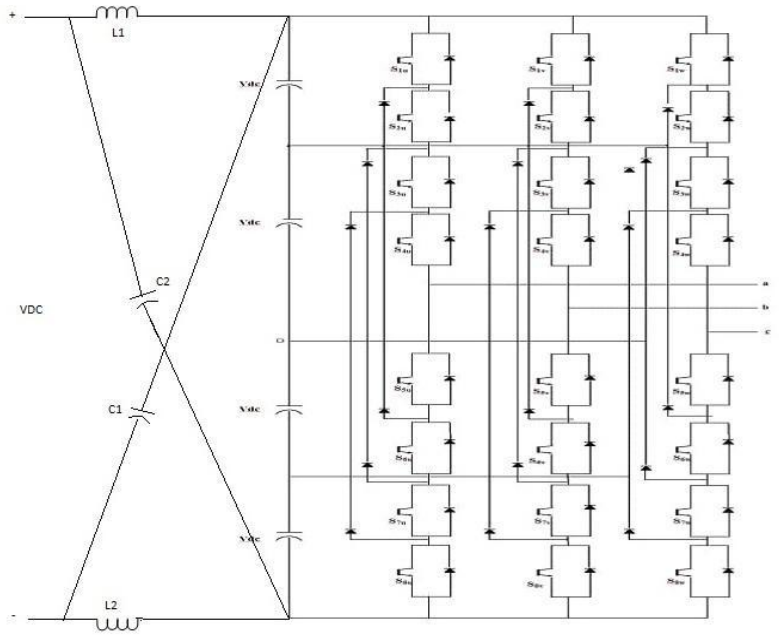

Fig.2. Five level diode clamped multilevel inverter.

TABLE II
Five-level switching sequences

Terminal voltages	Switching sequences							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
$+2v_{dc}$	On	On	On	On	Off	Off	Off	Off
$+v_{dc}$	Off	On	On	On	On	Off	Off	Off
0	Off	Off	On	On	On	On	Off	Off
$-v_{dc}$	Off	Off	Off	On	On	On	On	Off
$-2v_{dc}$	Off	Off	Off	Off	On	On	On	On

III. Control Techniques of Multilevel Inverter

Multicarrier PWM techniques involves the natural sampling of single modulating reference waveform typically being sinusoidal, through several carrier signals typically being triangular waveforms This modulation method is the logical extension of sine-triangle PWM for multilevel inverters, in which (m-1) carriers are needed for m-level inverter. They are

arranged in vertical shifts in continuous bands defined by the levels of the inverter. Each carrier has the same frequency and amplitude. A single voltage reference is compared to the carrier arrangement and the generated pulses are associated to each switching devices.

3.1Phase Disposition (PD)

This technique involves a number of carriers (m-l) which are all in phase accordingly. In 5 -level inverter all the four carrier waves are in phase with each other and compared with reference signal. According to that, the gate pulses are generated and are associated to each switching devices. The phase disposition PWM technique is illustrated in Fig. 3

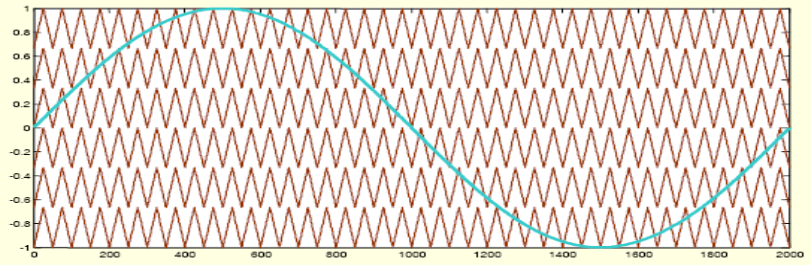

Fig.3. Phase disposition PWM technique

3.2. Phase Opposition Disposition (POD)

This technique employs a number of carriers (m-1) which are all in phase above and below the zero reference. In 5-level converters all the four carrier waves are phase shifted by 180 degrees between the ones above and below zero reference. The reference signal is compared with all four carrier waves there by gate pulses are generated and are associated to each switching devices. The phase opposition disposition PWM technique is illustrated in Fig.4.

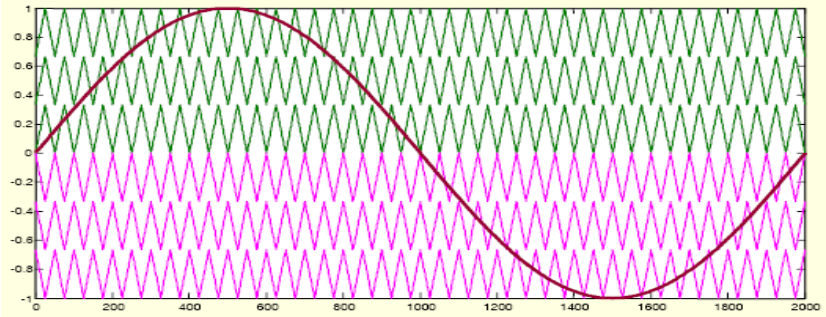

Fig.4. Phase opposition disposition PWM technique

3.3. Alternative Phase opposition Disposition (APOD)

This technique requires number of carriers (m-1) which are all phase displaced from each other by 180 degrees alternatively. The alternative phase opposition disposition PWM technique is illustrated in Fig. 5.

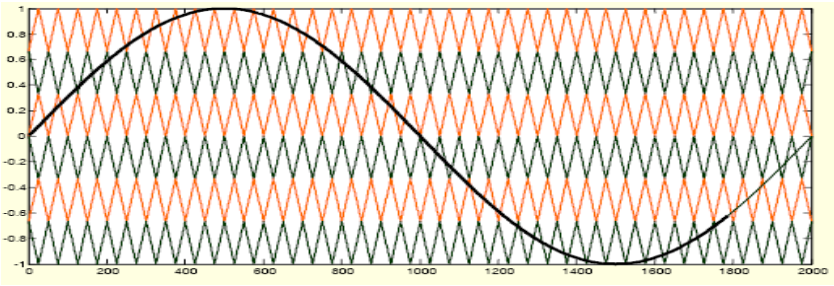

Fig.5. Alternative phase opposition disposition.

3.4. Phase Shift (PS)

This technique employs a number of carriers (m-l) phase shifted by 90 degree accordingly. In 5 -level converter all the four carrier waves are phase shifted by 90 degree. The phase shifted PWM technique is illustrated in Fig. 6.

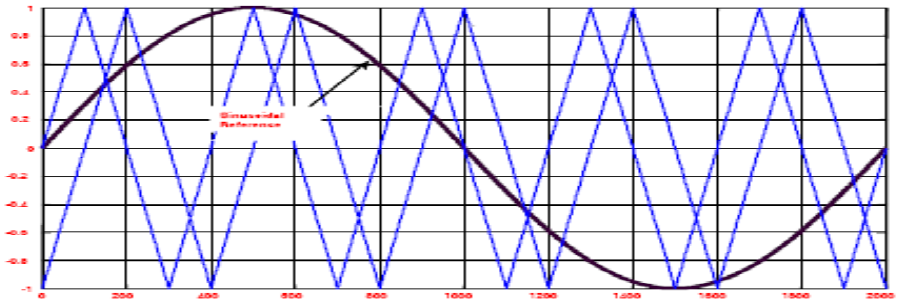

Fig.6. Phase shifted PWM technique.

IV. Simulation Results

Three level diode clamped multilevel inverter consist of 12 MOSET switches 6 clamping diodes and 2 DC link capacitor are connected with single DC source. Five level diode clamped multilevel Z-source inverter consist of 24 MOSET switches 12 clamping diodes and 4 DC link capacitor are connected with single DC source. The figure 7 and 9 shows the output voltages of 3-level and 5-Level respectively. THD values of 3-level neutral clamped multilevel inverter with PWM technique as illustrated in Fig.8. THD values of different multicarrier PWM techniques are shown in figure 10 to 13.

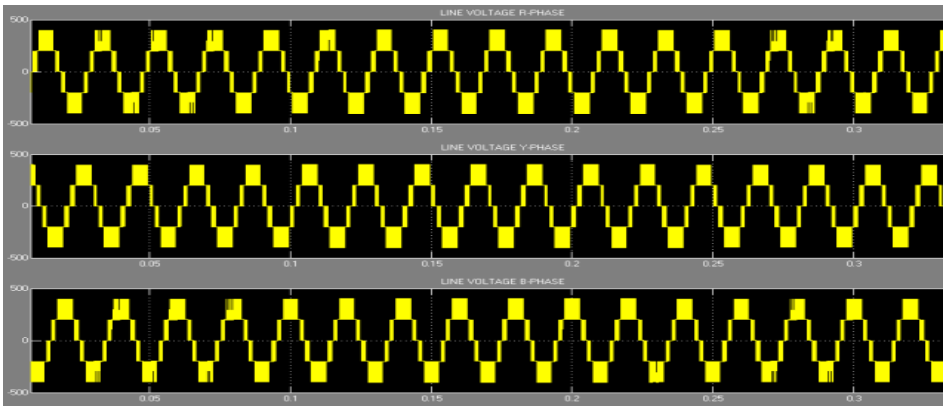

Fig.7. Line voltages of three level diode clamped multilevel inverter.

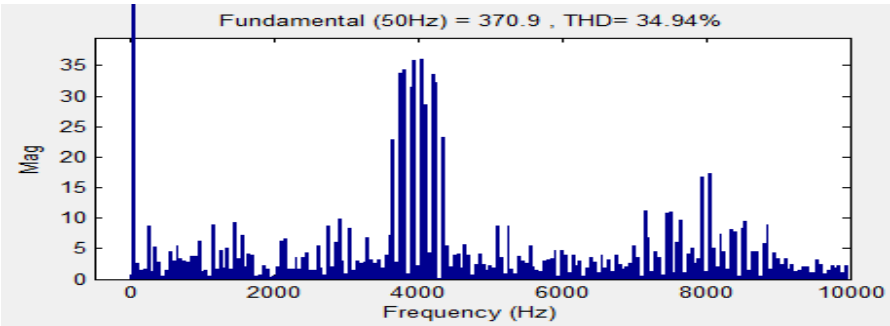

Fig.8. THD values of three level diode clamped multilevel Inverter with PWM technique.

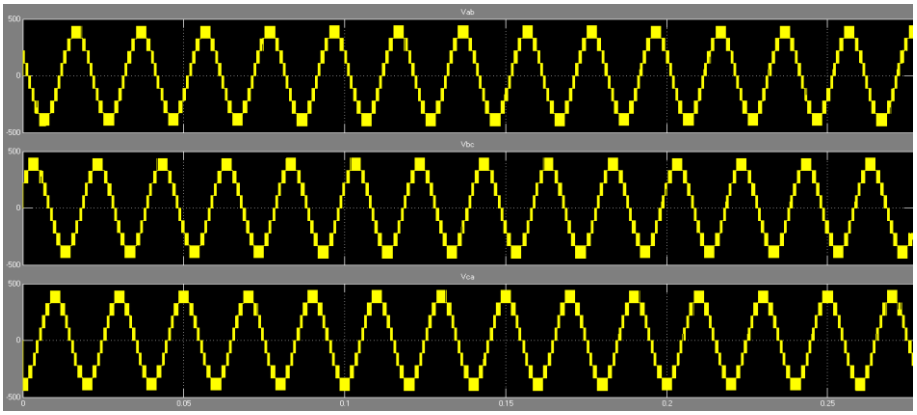

Fig.9. Line voltages of five level diode clamped multilevel z-source inverter.

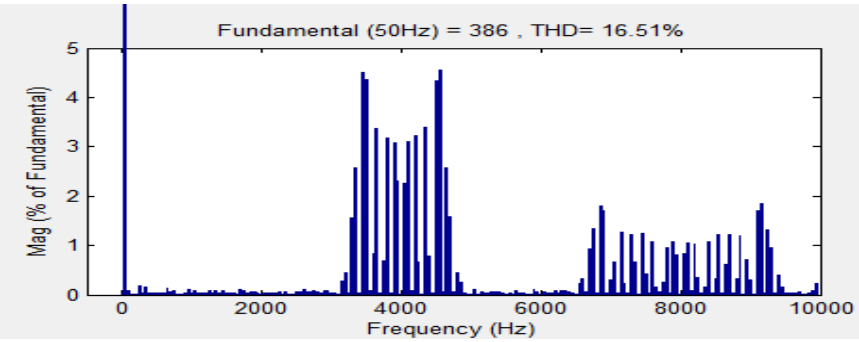

Fig .10.THD values of phase disposition PWM technique

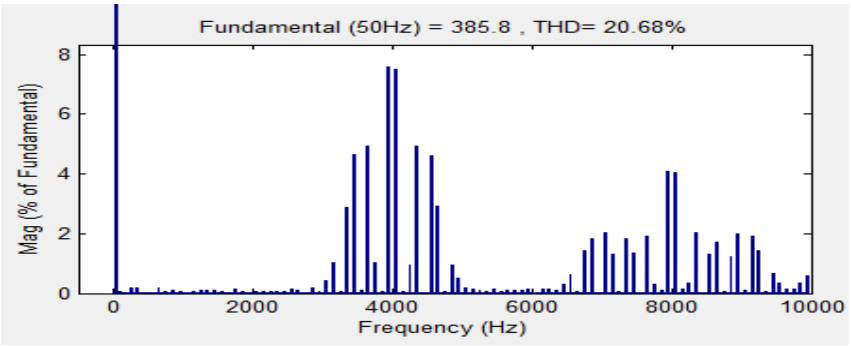

Fig.11. THD values of phase opposition disposition PWM technique.

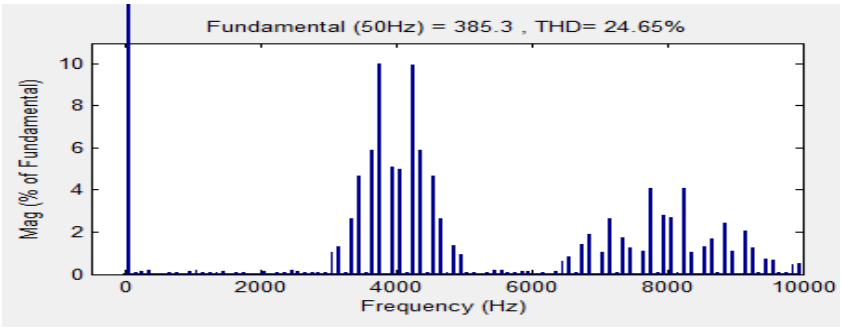

Fig.12. THD values of alternative phase opposition disposition PWM technique.

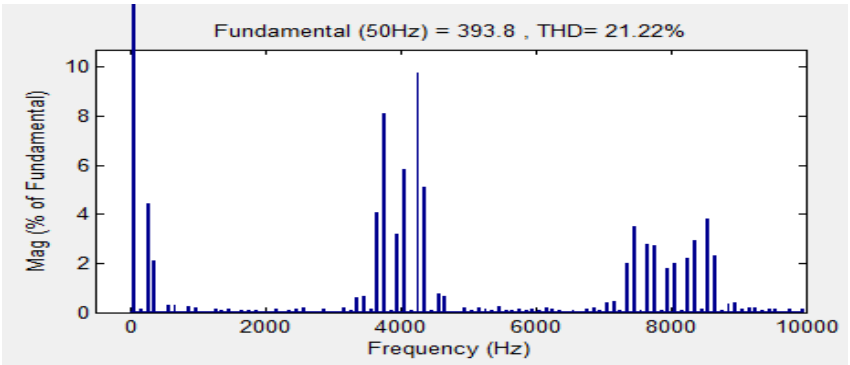

Fig.13. THD values of phase shifted PWM technique.

TABLE III
% OF THD VALUES

PWM TECHNIQUES	Three level DCMLI (%THD)	Five level DCMLI (%THD)
PD	34.94%	16.51%
POD	31.50%	20.68%
APOD	31.50%	24.65%
PS	57.12%	21.22%

V. Conclusion

The comparative THD analysis of a three phase five level diode clamped multilevel Z-source inverter is performed using various multicarrier PWM techniques. In proposed converter, Phase Disposition (PD), Phase Opposition Disposition (POD), Alternative Phase Opposition Disposition (APOD) and Phase Shifted (PS) PWM techniques are applied**.** The THD values of the output voltages of above mentioned techniques are compared with each other. From the above analysis, it is absorbed that the phase shifted PWM technique has less harmonic content in the output phase voltage compared with other multicarrier PWM control techniques and the proposed work has compared to the conventional three level inverter with PWM techniques by using MATLAB/SIMULINK.

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