Design and Implementation of Truncated Multipliers for Precision Improvement and Its Application to a Filter Structure

R. Devarani, [1] Mr. C.S. Manikanda Babu, [2]

1, 2(ECE-PG, Sri Ramakrishna Engineering College/ Anna University, Chennai, India)

ABSTRACT: *Truncated multipliers offers significant improvements in area, delay, and power. The proposed method finally reduces the number of full adders and half adders during the tree reduction. While using this proposed method experimentally, area can be saved. The output is in the form of LSB and MSB. Finally the LSB part is compressed by using operations such as deletion, reduction, truncation, rounding and final addition. In previous related papers, to reduce the truncation error by adding error compensation circuits. In this project truncation error is not more than 1 ulp (unit of least position). So there is no need of error compensation circuits, and the final output will be précised. To further extend the work the design is realized in a FIR filter.*

Keywords: *Computer arithmetic, faithful rounding, fixed- width multiplier, tree reduction, and truncated multiplier.*

I. INTRODUCTION

MULTIPLICATION is one of the most area consuming arithmetic operations in high-performance circuits. As a consequence many research works deal with low power design of high speed multipliers. Multiplication involves two basic operations, the generation of the partial products and their sum, performed using two kinds of multiplication algorithms, serial and parallel.

Serial multiplication algorithms use sequential circuits with feedbacks: inner products are sequentially produced and computed. Parallel multiplication algorithms often use combinational circuits and do not contain feedback structures. Multiplication of two bits produces an output which is twice that of the original bit.

It is usually needed to truncate the partial product bits to the required precision to reduce area cost. Fixed-width multipliers, a subset of truncated multipliers, compute only n most significant bits (MSBs) of the 2n-bit product for n × n multiplication and use extra correction/compensation circuits to reduce truncation errors. In previous related papers, to reduce the truncation error by adding error compensation circuits. So that the output will be précised.

In this approach jointly considers the tree reduction, truncation, and rounding of the PP bits during the design of fast parallel truncated multipliers so that the final truncated product satisfies the precision requirement. In our approach truncation error is not more than 1ulp (unit of least position), so there is no need of error compensation circuits, and the final output will be précised.

II. REDUCTION SCHEMES OF PARALLEL MULTIPLIERS

PP (partial product) generation produces partial product bits from the multiplicand and multiplier. PP reduction is used to compress the partial product bits to two. Finally the partial products bits are summed by using carry propagate addition.
1. Dadda tree
2. Wallace tree

Dadda reduction performs the compression operation whenever it required. Wallace tree reduction always compresses the partial product bits. In the proposed method, uses RA reduction method. So that the final bit will be reduced. In the proposed truncated multiplier design, introduces column-by-column reduction. Here two reduction schemes are used, to minimize the half adders in each column because the full adder has high compression rate when compared to HA.

2.1 Scheme1 and Scheme2
Fig. 1 shows the reduction procedure of Scheme 1, reduction starting from the least significant column. Column height is h, including the carry bits from least significant columns, are also shown on the top row where the columns that need HAs are highlighted by square boxes. Fig. 2 shows the RTL schematic of scheme 1 using Mentor Graphics.
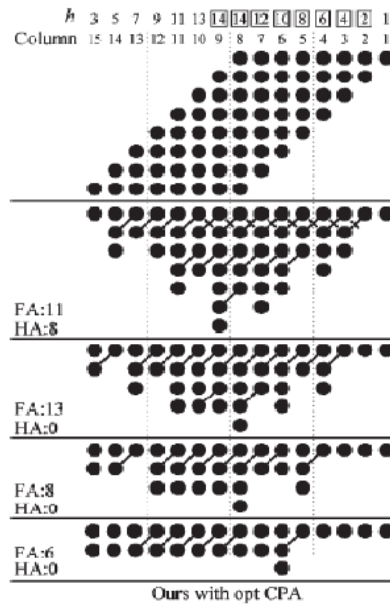
Fig. 1 Shows reduction procedure of scheme1 (38 FAs and 8 HAs).

Fig. 2 RTL schematic of scheme 1 using Mentor Graphics.

Scheme 1 having minimum CPA (carry propagate addition) bit width as twice reduction efficiency when compared to the Wallace method which produces the same result as that of RA method. Fig. 3 Shows reduction procedure of scheme 2. Scheme 1 is only used to determine whether an HA is needed and how many FAs are required in the per-column reduction that does not exceed the maximum number of Carry Save Additions in reduction levels.

The scheme1, scheme2 and proposed multiplier architecture has been simulated and synthesized using XILINX ISE Design Suite 8.1. From the synthesized results, the scheme 1 and scheme 2 has 1056 and 822 number of gates. The proposed multiplier has only 582 gates. Area utilization by the proposed method is less when compared to scheme 1 and scheme 2. Fig. 4 RTL schematic of scheme 2 using Mentor Graphics.
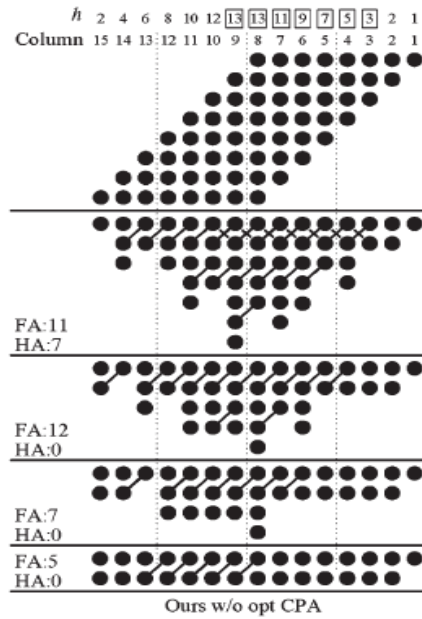
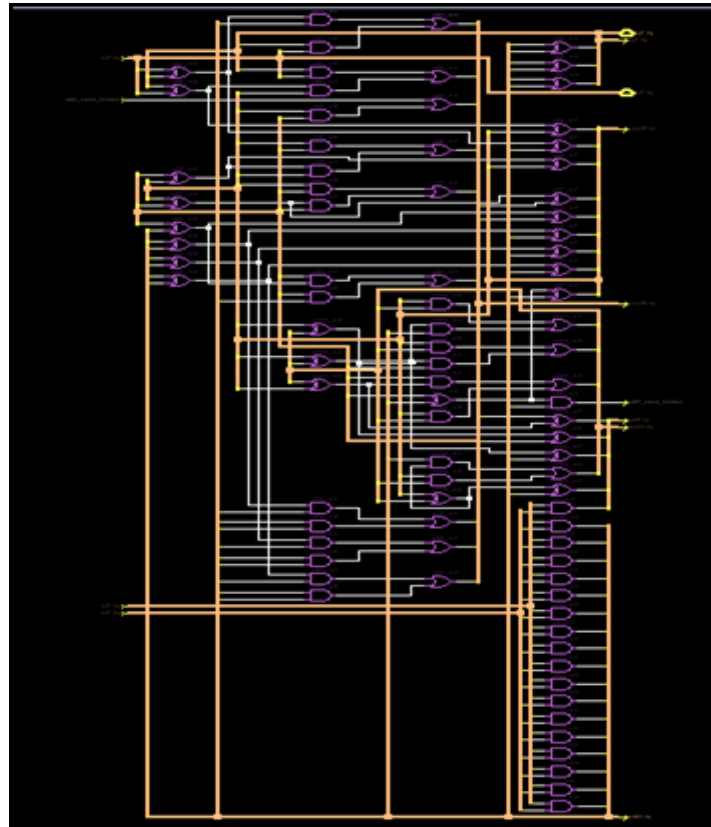Fig. 3 Shows reduction procedure of scheme 2(35 FAs and 7 HAs).

Fig. 4 RTL schematic of scheme 2 using Mentor Graphics.

III. PROPOSED PRECISION TRUNCATED MULTIPLIER DESIGN

The objective of a good multiplier is to provide a physically compact, good speed and low power consuming chip. To save significant power consumption of a VLSI design. In a truncated multiplier, several of the least significant columns of bits in the partial product matrix are not formed. This reduces the area and power consumption of the multiplier. It also reduces the delay of the multiplier in many cases, because the carry propagate adder producing the product can be shorter.

3.1 Deletion, Reduction, and Truncation of partial product bits

In the first step deletion operation is performed, that removes all the avoidable partial product bits which are shown by the light gray dots (fig 5). In this deletion operation, delete as many partial product bits as possible. Deletion error E_D should be in the range $-1/2$ ulp $\leq E_D \leq 0$.Hereafter, the injection correction bias constant of ¼ ulp.

The deletion error after the bias adjustment $-1/4$ ulp $\leq E_D \leq 1/4$ ulp. In Fig. 5, the deletion of partial product bits starts from column 3 by skipping the first two of partial product bits. After the deletion of partial product bits, perform column-by-column reduction of scheme 2.
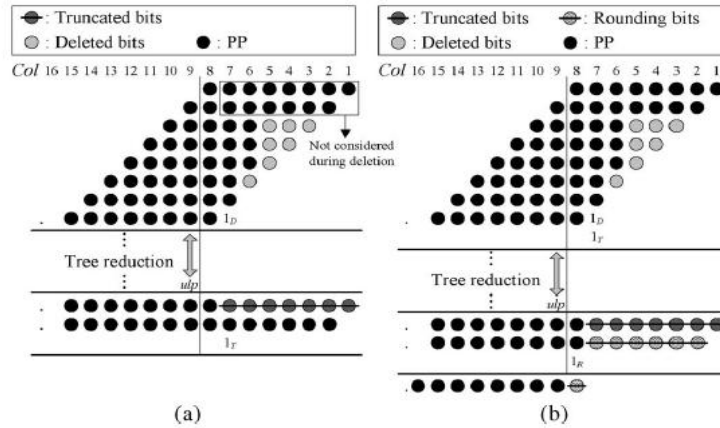

Fig. 5 8x8 truncated multiplication.(a) deletion, reduction and truncation. (b)deletion, reduction, truncation, and final addition.

After the reduction, perform the truncation, which will further removes the first row of (n-1) bits from column 1 to column (n-1). It will produces the truncation error which is in the range of $-1/2$ ulp $\leq E_T \leq 0$. Hence introduction of another bias constant of ¼ ulp in truncation part. So the adjusted truncation error is $-1/4$ ulp $\leq E_T \leq 1/4$ ulp.

3.2 Rounding and Final Addition

All the operations (deletion, reduction, and truncation) are done, finally the PP bits are added by using CPA (carry propagate addition) to generate final product of P bits. Before the final CPA, add a bias constant of   ½ ulp for rounding. Rounding error is in the form of $- 1/2$ ulp $\leq E_R \leq 1/2$ ulp. The faithfully truncated multiplier has the total error in the form of $-\text{ulp} < E = (E_D + E_T + E_R) \leq \text{ulp}$.

3.3 Proposed Algorithm

In proposed architecture we can multiply 8x8 bits, and the bits are reduced in step by step manner. Deletion is the first operation performed in Stage 1 to remove the PP bits, as long as the magnitude of the total deletion error is no more than 2^{-P-1}.Then number of stages to reduce the final bit width without increasing the error.

In normal truncated multiplier design, the architecture produces the output with some truncation error. But in the proposed design of truncated multiplier the truncation error is not more than 1 ulp, so the precision of the final result is improved. Fig. 6 shows proposed truncated multiplier.
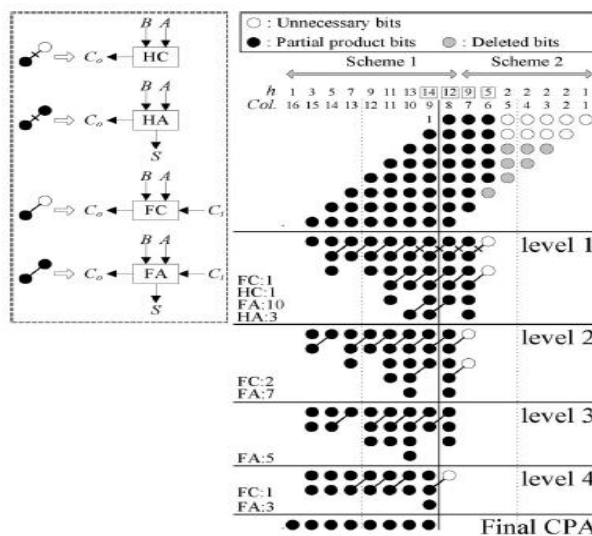

Fig. 6 Shows Proposed Truncated Multiplier.

IV. EXPERIMENTAL RESULTS

By using the Synthesis tool is Modelsim. The proposed system is implemented by using FPGA-Spartan 3E.This methods are mainly applicable in DSP systems.

4.1 Power and Area Analysis

TABLE 1 Power and Area analysis of the scheme 1, 2 & proposed

Parameter	Scheme 1	Scheme 2	Proposed
Power(W)	0.185	0.176	0.088
No. of Gate counts	1056	822	582

The scheme1, scheme2 and proposed multiplier architecture has been simulated and synthesized using XILINX ISE Design Suite 8.1. From the synthesized results, it is found that the scheme 1 consumes 185mW, scheme 2 consumes 176mW. The proposed multiplier consumes low power of 88mW when compared to scheme 1 and scheme 2.

The table 1 & 2 shows that the proposed method reduces the power and area than the previous methods. When compared to previous methods the precision is improved.

V. REALIZATION OF PROPOSED WORK IN FIR FILTER

Truncated multiplier can be effectively implemented in FIR filter structure. Conventional FIR filer performs ordinary multiplication of co-efficient and input without considers the length. Thus the structure can be made effective by replacing the existing multiplier with the proposed fixed width truncated multiplier for visible area reduction. Fig. 7 shows the architecture of FIR Filter.
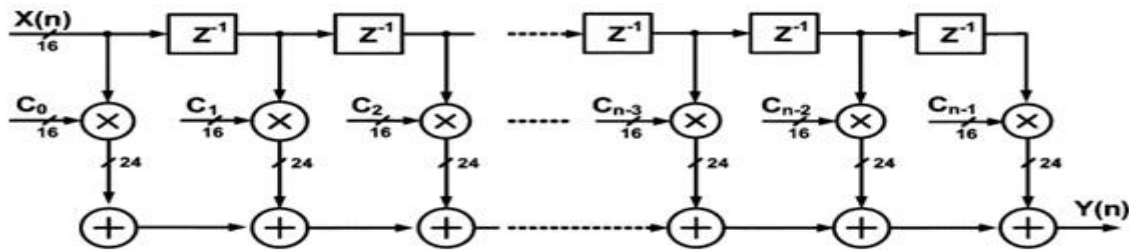
5.1 General FIR filter

Fig. 7 Architecture of FIR Filter.

Fig. 7 FIR filtering operation performs the weighted summations of input sequences, called as convolution sum, which are frequently used to implement the frequency selective—low-pass, high-pass, or band-pass filters. Generally, since
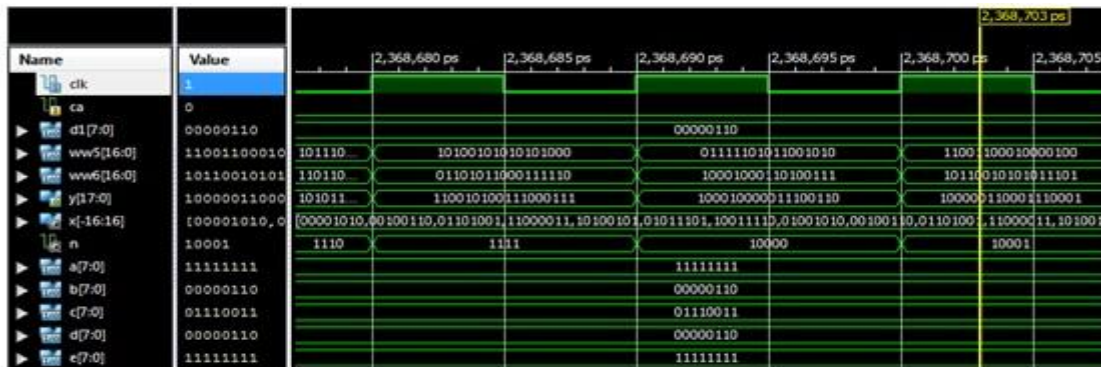

Fig. 8 Simulation Result of Conventional FIR Filter.

The amount of computation and the corresponding power consumption of FIR filter are directly proportional to the filter order, if we can dynamically change the filter order by turning off some of multipliers, significant power savings can be achieved.

However, performance degradation should be carefully considered when we change the filter order. The simulation result of conventional digital filter is shown in Fig. 8. The CLK represents the clock signal. The output is represented as the y. The coefficients are stored in the ROM as they are fixed. The n represents the tap of the filter. The output y changes with respect to the CLK signal.

The power of the conventional FIR filter is analyzed by using XILINX power analyzer . The power calculated with respect to the CLK.

TABLE 2 Area analysis of conventional FIR filter

Parameter	Conventional
No. of Gate counts	22,362

5.2 Modified FIR filter

The proposed work is implemented in FIR filter structure, where the results of the FIR structure with fixed width multipliers show considerable area reduction when compared to conventional FIR filter. Fig. 9 shows the area analysis result of modified FIR filter. Fig. 11 shows the power analysis of modified FIR filter. The power is also reduced due to the effectiveness of the design. Fig. 10 shows the simulation result of modified FIR filter.
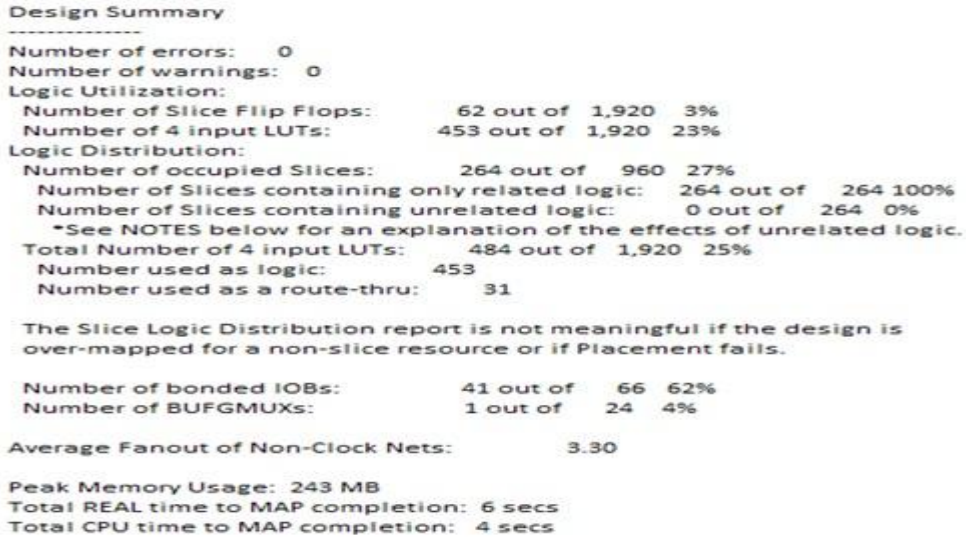

Fig. 9 Area analysis of modified FIR filter.
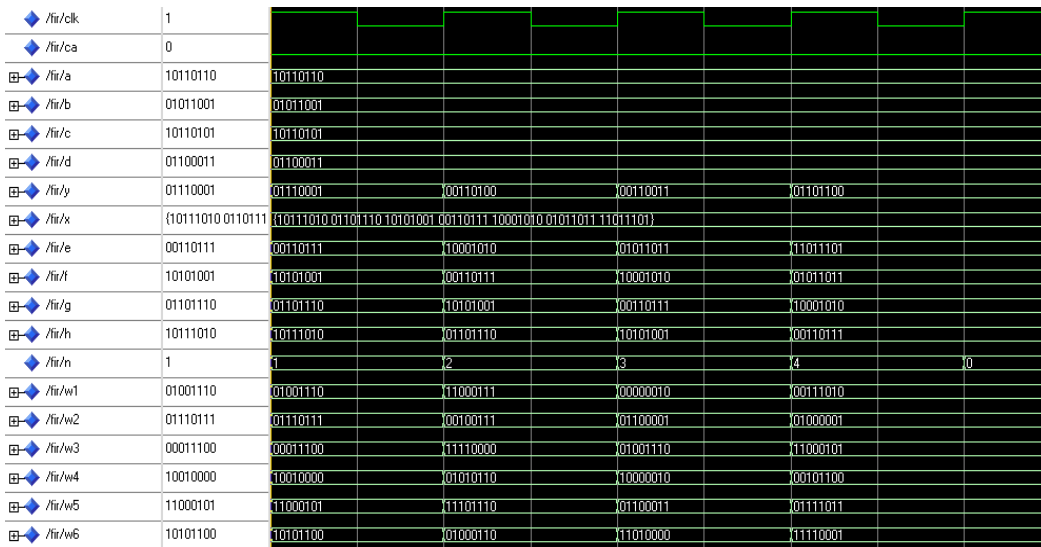

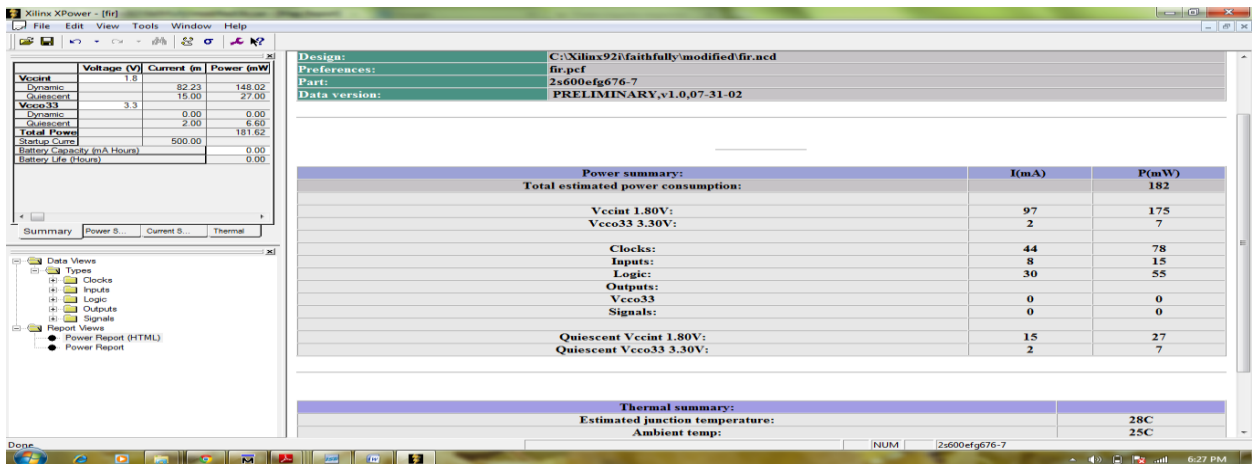Fig. 10 Simulation result of modified FIR filter.

Fig. 11 Power analysis of modified FIR filter.

VI. CONCLUSION

There are many works proposed to reduce the truncation error by adding error compensation circuits so as to produce a précised output. This approach jointly considers the tree reduction, truncation, and rounding of the PP bits during the design of fast parallel truncated multipliers, so that the final truncated product satisfies the precision requirement.

In this approach truncation error is not more than 1ulp, so there is no need of error compensation circuits, and the final output will be précised. The scheme1, scheme2 and proposed multiplier architecture has been simulated and synthesized using XILINX ISE Design Suite 8.1.

From the synthesized results, it is found that the scheme 1 consumes 185mW, scheme 2 consumes 176mW. The proposed multiplier consumes low power of 88mW when compared to scheme 1 and scheme 2. The scheme 1and scheme 2 has 1056 and 822 number of gates. The proposed multiplier has only 582 gates. Area utilization by the proposed method is less when compared to scheme 1 and scheme 2.

The proposed work is implemented in FIR filter structure, where the results of the FIR structure with fixed width multipliers show considerable area reduction. The power is also reduced due to the effectiveness of the design.

VII. ACKNOWLEDGEMENTS

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