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Performance Evaluation of Single Phase H-Bridge Type Diode Clamped Five Level Inverter

E.Sambath[1], S.P. Natarajan[2], C.R.Balamurugan[3]
[1,2]*Department of EIE, Annamalai University, Chidambaram, Tamilnadu, India*
[3]*Department of EEE, Arunai Engineering College, Thiruvannamalai, Tamilnadu, India*

ABSTRACT
The Diode Clamped Multilevel Inverter (DCMLI) is an attractive type multilevel inverter due to its robustness. This paper discusses new modulation strategies for a single phase five level H-bridge type DCMLI with reduced components as compared to conventional DCMLI. The chosen multi level inverter is controlled with multicarrier based Sinusoidal Pulse Width Modulation (SPWM) technique with Variable Frequency (VF), Phase Shift (PS), Carrier Overlapping (CO), Phase Opposition and Disposition (POD), Alternative Opposition and Disposition (APOD) and Phase Disposition (PD) PWM techniques. The performance of proposed strategies are evaluated through MATLAB-SIMULINK/POWER SYSTEM BLOCKSET / POWER GUI. The variation of Total Harmonic Distortion (THD), V_{RMS} (fundamental), Form Factor (FF), Crest Factor (CF) and Distortion Factor (DF) are observed for various modulation indices. The simulation results indicates that sinusoidal reference with PODPWM/APODPWM provides output with relatively low distortion. It is also seen that COPWM strategy is found to perform better since it provides relatively higher fundamental RMS output voltage.

Keywords **: COPWM , DCMLI, DF, SH PWM, THD**

I. INTRODUCTION

A Multi Level Inverter (MLI) can switch either its input or output nodes (or both) between multiple (more than two) levels of voltage or current. As the number of levels reaches infinity, the output THD approaches zero. The number of the achievable voltage levels however is limited by voltage imbalance problems, voltage clamping requirements, circuit layout and packaging constraints, complexity of the controller and of course, capital and maintenance costs. Three different major multilevel inverter structures have been applied in industrial applications: Cascaded H-bridge inverter with Separate DC sources(SDCS), diode clamped inverter and flying capacitors inverter. Yuan and Barbi [1] proposed fundamentals of a new diode clamping multilevel inverter. Anshuman Shukla et al [2] introduced control schemes for equalization of DC capacitor voltage in diode clamped multilevel inverter. Deepthi and Saxena [3] havediscussed variation of THD in a diode clamped multilevel inverter with respect to modulation index and control strategy. NagaHaskar Reddy et al [4] have proposed a advanced modulating technique for diode clamped multilevel inverter fed induction motor. Jose Rodriguez et al [5] have presented a survey of multilevel inverters topologies, controls and applications. Yu Liu et al [6] found a new clew for research on realtime algorithm for minimizing THD in multilevel inverters with unequal or varying voltage steps under staircase modulation. Hinago and Koizumi [7] proposed single phase multilevel inverter using switched series/parallel DC voltage sources. Xue and Manjrekar [8] developed a new class of single phase multilevel inverter. Farokhnia et al [9] made a comparison between approximate and accurate line voltage THD of multilevel inverter with equal DC sources. Farokhnia et al [10] also made a comparison between approximate and accurate calculation of line voltage THD in multilevel inverters with unequal DC sources. Rahim and Selvaraj [11] proposed multistring five level inverter with novel PWM control scheme for photo voltaic application. Shanthi and Natarajan [12] have described that the multilevel inverter triggered by the developed unipolar PWM strategies exhibits reduced harmonics and higher DC bus utilisation. PWM strategies developed are implemented in real time using dSPACE/Real Time Interface (RTI).Seyezhai [13] presented carrier overlapping PWM methods for asymmetrical multi level inverter. This literature survey reveals few papers only on various PWM techniques and DCMLI. Hence this work presents a new approach for controlling the harmonics of output voltage of chosen DCMLI fed resistive load employing sinusoidal switching reference. Simulations are performed using MATLAB-SIMULINK.

II. MULTILEVEL INVERTER

The operation of a multilevel inverter can be described as an optional stacking of a number of DC voltage source stages dependent on a certain time of operation that one stage is stacked (forward or reverse) or bypassed MLIs also have some issues, such as requiring a big number of semiconductor switches which increases as the number of steps/levels increases and complex design for synchronous gate drivers for different levels. There are many types of multilevel inverter topologies in its history, starting from the series H-bridge design, followed by the diode-clamped, which utilizes a bank of capacitors to split the DC bus voltage and then the switched flying capacitor (or capacitor clamped) topology. An inverter design can also cascade these fundamental topologies to make hybrid topologies to improve power quality.

II. (a) Conventional DCMLI

The main concept of this inverter is to use diodes to limit the voltage stress on power devices. A DCMLI typically consists of (m-1) capacitors on the DC bus where m is the total number of positive, negative and zero levels in the output voltage. The order of numbering of the switches is S1, S2, S3, S4, S1', S2', S3' and S4'. The DC bus consists of four capacitors C1, C2, C3 and C4 acting as

voltage divider. For a DC bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$ and voltage stress on each device is limited to $V_{dc}/4$ through clamping diode. The middle point of the four capacitors 'n' can be defined as the neutral point. The principle of diode clamping to DC link voltages can be extended to any number of voltage levels. Since the voltages across the semiconductor switches are limited by conduction of the diodes connected to the various DC levels, the inverter is called DCMLI. The switches are arranged into 4 pairs (S1,S1'), (S2,S2'), (S3,S3') and (S4,S4'). If one switch of the pair is turned ON, the complementary switch of the same pair must be OFF. The output voltage V_{an} has five states: $V_{dc}/2$, $V_{dc}/4$, 0, - $V_{dc}/4$ and - $V_{dc}/2$. Four switches are triggered at any point of time to select the desired level in the five level DCMLI. Fig.1 shows a conventional single phase one leg five level DCMLI.

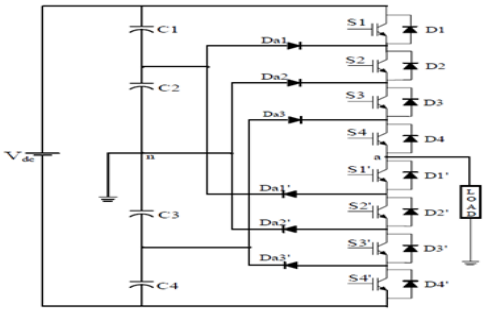

Figure 1 Conventional single phase five level DCMLI

II. (b) Chosen DCMLI

Two important issues in multilevel inverter control are obtaining near sinusoidal output voltage waveform and the elimination of the lower order harmonics. In this paper, a H-bridge type diode clamped inverter is used to propose a modified switching technique in such a way that the THD and number of components is minimized. Table 1 shows that comparisons of components used in conventional as well as chosen DCMLI. Fig.2 shows a configuration of single phase five level H-bridge type DCMLI. Here also the same output voltage states exist : $V_{dc}/2$, $V_{dc}/4$, 0, - $V_{dc}/4$ and - $V_{dc}/2$. The gate signals used for five level H-bridge type DCMLI are simulated using MATLAB – SIMULINK / POWER SYSTEM BLOCKSET / POWER GUI. The gating pulses for the inverter are generated for various values of modulation index m_a and for various PWM techniques. The chosen DCMLI is investigated with multicarrier SPWM for modulation indices ranging from 0.6-1.

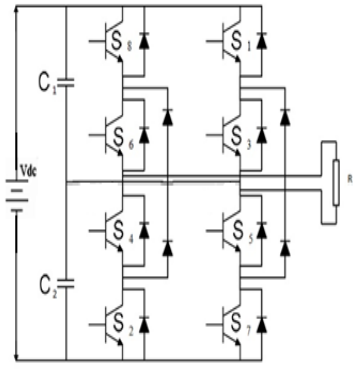

Figure 2 Chosen single phase H-bridge type five level DCMLI

TABLE-1
Comparison between conventional DCMLI and chosen DCMLI

Type of MLI	Conventional DCMLI	Chosen DCMLI
Main power devices	8	8
Main diodes	8	8
Clamping diodes	6	4
DC bus capacitors	4	2
Balancing capacitors	0	0
No. of leg	1	2

III. MODULATION TECHNIQUE FOR SWITCHES

In this paper a control technique of carrier based SPWM strategy is present. Number of triangular waveforms is compared with a controlled sinusoidal modulating signal. The number of carriers required to produce the m- level output is m-1. All the carriers have the same peak to peak amplitude A_{cpp}. The reference is continuously compared with each of the carrier signals and whenever the reference is greater then the carrier signal, the pulse is generated. The switching rules for the switches are decided by the intersection of the carrier waves with the modulating signal. The frequency modulation index $m_f=f_c/f_o$ where f_c is the frequency of the carrier signal and f_o is the frequency of the modulating signal. The amplitude modulation index is m_a where A_0 is the amplitude of the modulating signal and A_{cpp} is the peak to peak value of the carrier (triangular) signal. The amplitude modulation indices are :

SHPWM and VFPWM = $2A_o/(m-1).A_{cpp}$
COPWM = $A_o/(m/4).A_{cpp}$
PSPWM = $A_o/(A_{cpp}/2)$

Multiple degrees of freedom are available in carrier based multilevel PWM. The principle of the carrier based PWM strategy is to use m-1 different carriers with a reference signal for a m level inverter. Differences of carriers includes carrier's frequency, carrier's amplitude, carrier's phases , carrier's DC offset and multiple third harmonic content of reference signal. This paper uses different modulation strategies that all well known carrier based multilevel PWM strategies such as PDPWM, PODPWM, APODPWM, COPWM, PSPWM and VFPWM. Fig.3 shows the sample SIMULINK model developed for PSPWM technique for chosen inverter.

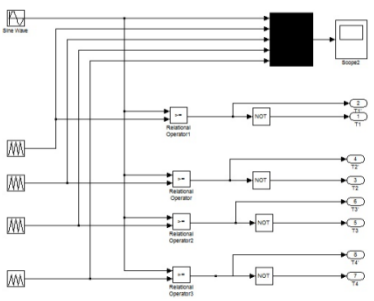

Figure 3 Sample SIMULINK model developed for chosen single phase inverter for PSPWM technique

III. (a) Phase Disposition PWM (PDPWM) Strategy

In this method all carriers have the same frequency, amplitude and phases but they are just different in DC offset to occupy contiguous bands. Since all carriers are selected with the same phase, the method is known as PD strategy. The carrier arrangement for this strategy is shown in Fig.4.

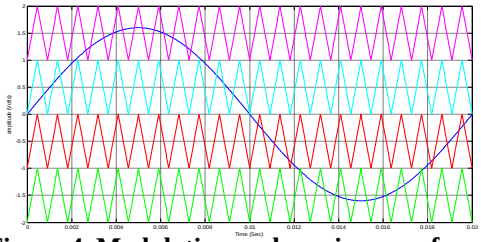

Figure 4 Modulating and carrier waveforms for PDPWM strategy (m_a=0.8 and m_f=22)

III. (b) Phase Opposition Disposition PWM (PODPWM) Strategy

The PODPWM strategy is having the carriers above the zero line of reference voltage out of phase with those of below the line by 180 degrees as shown in Fig.5.

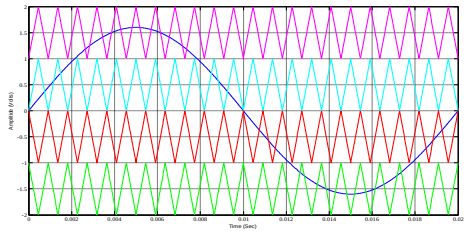

Figure 5 Modulating and carrier waveforms for PODPWM strategy (m_a=0.8 and m_f=22)

III. (c) Alternative Phase Opposition and Disposition PWM (APODPWM) Strategy

In APOD strategy each carrier is phase shifted by 180 degrees from its adjacent one as shown in Fig.6.

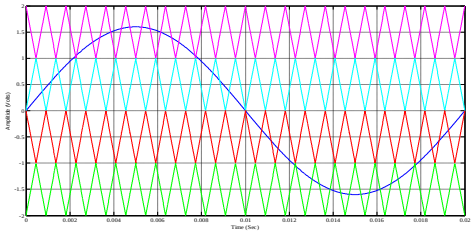

Figure 6 Modulating and carrier waveforms for APODPWM strategy (m_a=0.8 and m_f=22)

III. (d) Phase Shift PWM (PSPWM) Strategy

In this strategy all carrier signals have the same amplitude and frequency but they are phase shifted by 90 degrees to each other as shown in Fig.7.

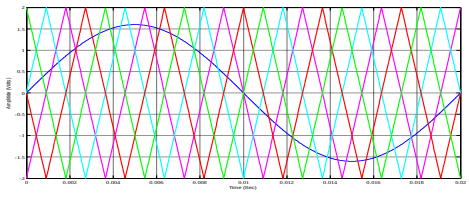

Figure 7 Modulating and carrier waveforms for PSPWM strategy (m_a=0.8 and m_f=22)

III. (e) Carrier Overlapping PWM (COPWM) Strategy

For an m-level inverter, m-1 carriers with the same frequency f_c and same peak to peak amplitude A_{cpp} are disposed such that the bands they occupy overlap each other. The overlapping vertical distance between each carrier is A_{cpp} /2 which is shown in Fig.8. The reference waveform has amplitude of A_o and frequency f_o and it is centred in the middle of the carrier signals.

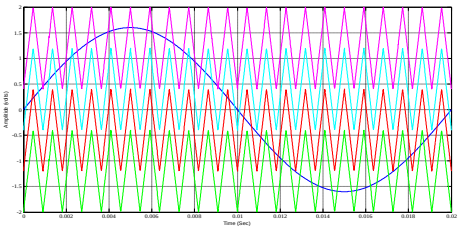

Figure 8 Modulating and carrier waveforms for COPWM strategy (m_a=0.8 and m_f=22)

III. (f) Variable Frequency PWM (VFPWM) Strategy

The number of switchings for upper and lower devices of chosen MLI is much more than that of intermediate switches in PDPWM using constant frequency carriers. In order to equalize the number of switchings for all the switches, variable frequency PWM strategy is used as illustrated in Fig.9 in which the carrier frequency of the intermediate switches is properly increased to balance the number of switchings for all the switches.

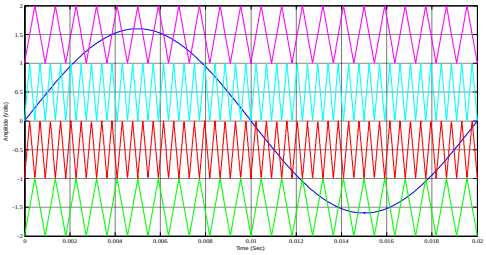

Figure 9 Modulating and carrier waveforms for VFPWM strategy (m_a=0.8 and m_f=22 for upper and lower switches)

IV. SIMULATION RESULTS

Simulation studies are performed by using MATLAB-SIMULINK to verify the proposed PWM strategies for chosen single phase H- bridge type diode clamped five level inverter for various values of m_a ranging from 0.6 – 1 and corresponding %THD values are measured using FFT block and they are shown in Table 2. Table 3 shows the V_{RMS} of fundamental of inverter output for the same modulation indices. Figs.10-21 show the simulated output voltage of chosen DCMLI and the corresponding FFT plots with different strategies but only for one sample value of m_a=0.8 and m_f=22. Fig.10 shows the five level output voltage generated by PDPWM strategy and its FFT plot is shown in Fig.16. From Fig.16, it is observed that the PDPWM strategy produces significant 12^{th},14^{th},18^{th} and 20^{th} harmonic energy. Fig.11 shows the five level output voltage generated by PODPWM strategy and its FFT plot is shown in Fig.17. From Fig.17, it is observed that the PODPWM strategy produces significant 15^{th},17^{th} and 21^{th} harmonic energy. Fig.12 shows the five level output voltage generated by APODPWM strategy and its FFT plot is shown in Fig.18.

From Fig.18, it is observed that the APODPWM strategy produces significant 17^{th},19^{th} and 21^{th} harmonic energy. Fig.13 shows the five level output voltage generated by PSPWM strategy and its FFT plot is shown in Fig.19. From Fig.19, it is observed that the PSPWM strategy produces significant 11^{th},17^{th} , 19^{th} and 21^{th} harmonic energy. Fig.14 shows the five level output voltage generated by COPWM strategy and its FFT plot is shown in Fig.20. From Fig.20, it is observed that the COPWM strategy produces significant 3^{rd} and 20^{th} harmonic energy. Fig.15 shows the five level output voltage generated by VFPWM strategy and its FFT plot is shown in Fig.21. From Fig.21, it is observed that the VFPWM strategy produces significant 16^{th} and 20^{th} harmonic energy.

The following parameter values are used for simulation : V_{DC}=440V ,f_c=1100Hz and R(load)=100 ohms.

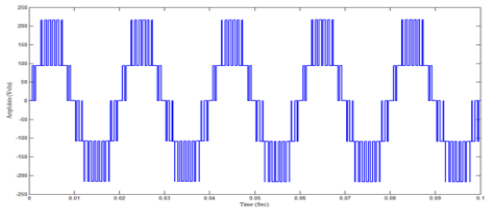

Figure 10 Simulated output voltage generated by PDPWM technique for R load

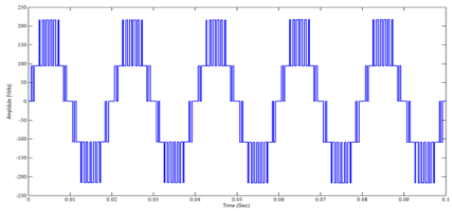

Figure 11 Simulated output voltage generated by PODPWM technique for R load

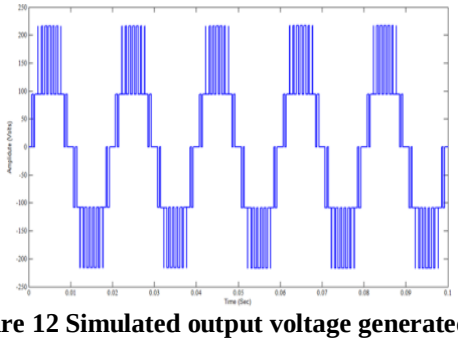

Figure 12 Simulated output voltage generated by APODPWM technique for R load

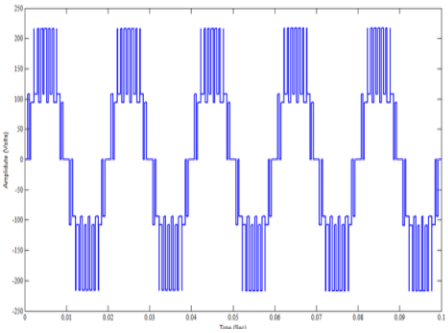

Figure 13 Simulated output voltage generated by PSPWM technique for R load

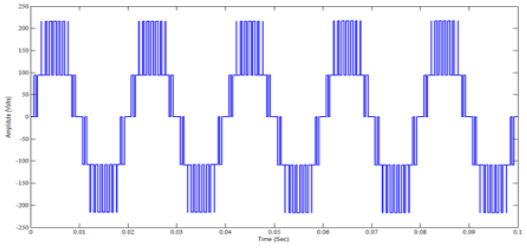

Figure 14 Simulated output voltage generated by COPWM technique for R load

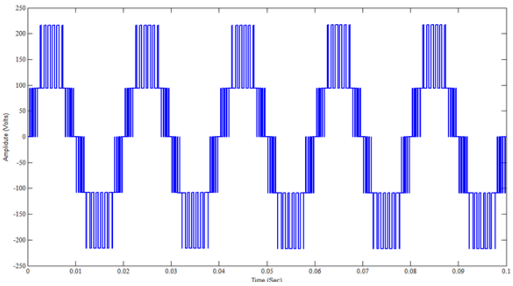

Figure 15 Simulated output voltage generated by VFPWM technique for R load

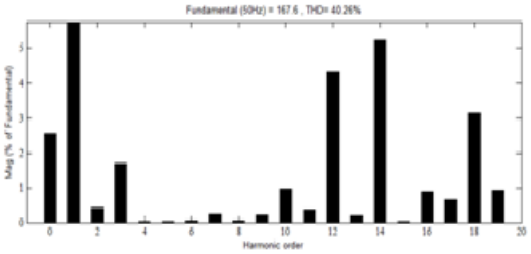

Figure 16 FFT spectrum for PDPWM technique

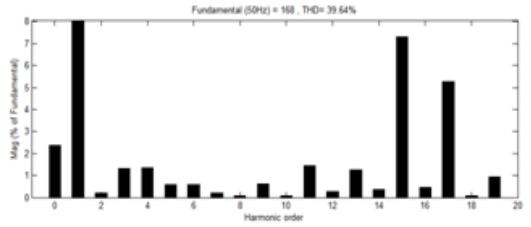

Figure 17 FFT spectrum for PODPWM technique

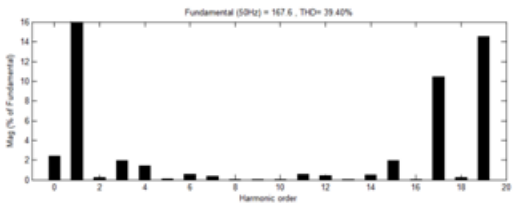

Figure 18 FFT spectrum for APODPWM technique

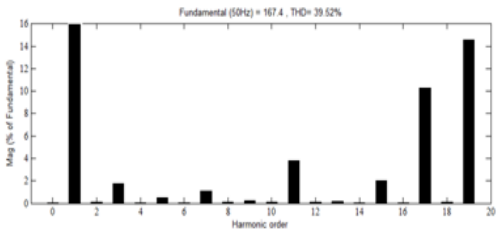

Figure 19 FFT spectrum for PSPWM technique

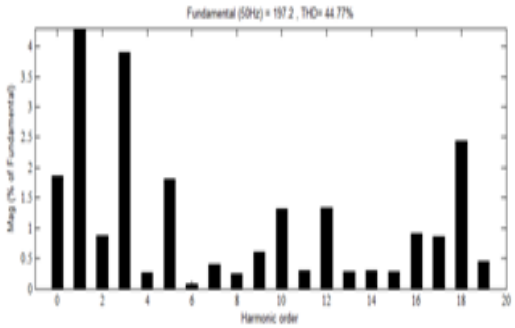

Figure 20 FFT spectrum for COPWM technique

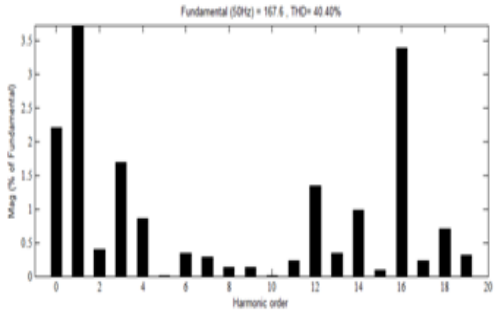

Figure 21 FFT spectrum for VFPWM technique

TABLE-2
%THD of output voltage of chosen DCMLI for various values of m_a

m_a	PD	POD	APOD	VF	CO	PS
1	27.91	27.66	27.70	27.94	34.03	27.70
0.9	34.69	34.38	34.94	34.96	39.09	35.03
0.8	40.26	39.64	39.40	40.40	44.77	39.52
0.7	44.04	43.60	43.60	44.09	51.22	43.81
0.6	45.87	44.87	44.51	46.05	60.50	44.84

TABLE-3
RMS (fundamental) of output voltage of chosen DCMLI for various values of m_a

m_a	PD	POD	APOD	VF	CO	PS
1	150.9	150.4	151	151	162.3	150.9
0.9	134.9	134.1	135	134.8	151.4	135
0.8	118.5	118.8	118.5	118.5	139.4	118.4
0.7	102.7	102.5	102.9	102.6	126.6	102.9
0.6	87.1	87.57	87.17	87.12	111.9	87.14

TABLE-4
CF of output voltage of chosen DCMLI for various values of m_a

m_a	PD	POD	APOD	VF	CO	PS
1	1.4141	1.414	1.4139	1.413	1.414	1.414
0.9	1.4143	1.414	1.414	1.413	1.414	1.414
0.8	1.4143	1.414	1.4144	1.414	1.414	1.413
0.7	1.4138	1.413	1.4139	1.414	1.414	1.413
0.6	1.4144	1.413	1.4144	1.414	1.414	1.413

TABLE-5
FF of output voltage of chosen DCMLI for various values of m_a

m_a	PD	POD	APOD	VF	CO	PS
1	79.421	113.93	21.3	98.69	174.51	5030
0.9	50.14	73.68	75.84	60.72	127.22	4500
0.8	46.47	49.707	49.37	53.86	74.54	2960
0.7	29.511	33.27	33.73	32.06	59.15	3430
0.6	22.5	23.004	22.7	21.78	48.23	4357

TABLE-6
DF of output voltage of chosen DCMLI for various values of m_a

m_a	PD	POD	APOD	VF	CO	PS
1	0.45	0.3329	0.2783	0.3345	0.82	1.998
0.9	0.4251	0.3152	0.2199	0.3191	0.722	0.1944
0.8	0.2372	0.1923	0.2485	0.2255	0.5211	0.212
0.7	0.3923	0.3043	0.3003	0.317	0.4181	0.1689
0.6	0.329	0.5077	0.5171	0.4156	0.4604	0.1283

V. CONCLUSION

Single phase H-bridge type diode clamped five level inverter employing different multi carrier single reference modulation schemes has been investigated. It is found from Table 2 that PODPWM /APODPWM techniques provide output with relatively low distortion. COPWM technique is observed to perform better since it provides relatively higher fundamental RMS output voltage (Table 3). Table 4 shows crest factor, Table 5 provide FF and Table 6 shows DF for all modulation indices.

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