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Design of DC–DC Converter with Fast Dynamic Response for Photovoltaic Sources

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Abstract: *This paper proposes a high efficiency dc-dc converter with fast dynamic response for low-voltage photovoltaic (PV) sources. The voltage stress of power switches is reduced by soft-switching operation at low voltage side. Zero current turn-off of output diodes is achieved at high voltage side. Full bridge converter is used at high voltage side to increase the output voltage. Filter is used to reduce ripples in the output. Inverter is also connected at high voltage side for ac applications. The dynamic response of the proposed converter is improved. The performance of the proposed converter is verified using Matlab-simulink.*

Index Terms: *DC–DC converter, dynamic response, photo-voltaic (PV).*

I. Introduction

The photovoltaic (PV) module-integrated converter (MIC) system is the key technology for the future distributed pro-duction of electricity using solar energy [1]–[3]. The PV MIC system offers "plug and play" concept, greatly optimizing the energy yield from the PV module [3]. Each PV module has its own power conversion system, generating the maximum power from the PV module [4]. To make the PV MIC system commer-cially viable, a low-cost and high-efficiency power conversion scheme should be developed.

The PV module voltage has a low-voltage characteristic [5]. In order to deliver electric power into the grid, the low PV module voltage should be converted into a high dc voltage [6]. Thus, a dc–dc converter with a high-voltage gain is needed. The active-bridge dc–dc converter has been used for low-voltage PV sources [7], [8]. The power switches at low-voltage side are turned ON at zero voltage. However, the output diode at high-voltage side has high switching power losses due to its reverse-recovery current [9]. The half-bridge dc–dc converter has been presented to reduce switching power losses at high-voltage side [10]. The output diodes are turned OFF at zero current by using the voltage doubler rectifier. However, an additional half-wave rectifier is needed, which increases switch-ing power losses. Alternatively, the active-clamped dc–dc con-verter has been used for low-voltage PV sources [11], [12]. It uses the active-clamping circuit and the resonant voltage dou-bler rectifier. However, the active-clamping circuit increases the voltage stress of power switches at low-voltage side, causing high switching power losses. Additionally, thermal manage-ment problems should be considered for a practical design of the PV MIC system.

Considering the dynamic response of the converter, band-width limitations of conventional controllers have forced power electronics engineers to increase switching frequency or in-crease output capacitor [13]. Such hardware modification results in lower efficiency and higher component cost. However, by improving the controller's dynamic response, the transient performance of the converter can be improved. Therefore, it is not only necessary but also practical to improve both power efficiency and dynamic response of the dc–dc converter for low-voltage PV sources. An improved active-clamped dc–dc converter is presented by using a dual active-clamping circuit. The voltage stress of power switches can be reduced at low-voltage side. The transient performance of the proposed con-verter is improved. Power efficiency is improved by reducing switching power losses [14].

This paper proposes design of dc-dc converter with fast dynamic response for photovoltaic sources. The voltage stress of power switches is reduced by soft-switching operation at low voltage side. Zero current turn-off of output diodes is achieved at high voltage side. Full bridge converter is used at high voltage side to increase the output voltage. Π filter is used to reduce ripples in the output. Inverter is also connected at high voltage side for ac applications. The dynamic response of the proposed converter is improved. The performance of the proposed converter is verified using Matlab-simulink .

II. Proposed Converter Configuration

Fig.1 shows the circuit diagram of the proposed dc-dc converter. The converter consists of main switches (S_1,S_4),the dual active –clamping circuit (S_2,S_3,C_c), the transformer T, and resonant voltage doubler rectifier. The main switches (S_1,S_4) and auxiliary switches (S_2,S_3) operate complementarily with a short dead time. All switches are the metal-oxide semiconductor field effect transistors. They are considered ideal switches except their body diodes D_{s1}-D_{s2} and output capacitors C_{s1}-C_{s4}.

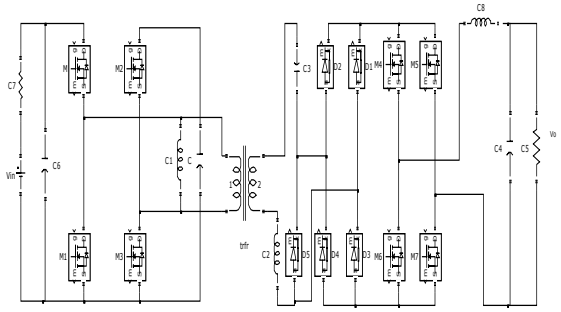

Fig.1 Proposed circuit diagram

C_i is the input capacitor. C_c is the clamping capacitor. C_o is the output capacitor. The capacitors C_i , C_c , and C_o are large enough so that their voltages V_i , V_c , and V_o are considered constant, respectively. The transformer T has the magnetizing inductor L_m and leakage inductor L_{lk} with the turns ratio of 1:N, where $N=N_s/N_p$. L_{lk} is assumed to be much smaller than L_m. The capacitor C_r is the resonant capacitor. C_r resonates with the leakage inductor L_{lk} . Thus, the resonant capacitor voltage V_r is not considered constant for one switching period. Fig 2. shows the switching waveforms of the proposed converter during one switching period T_s ($=1/f_s$). The proposed converter has six switching modes during T_s . The duty ratio D is based on the on-time of the main switches. Figure.3.3(a),(b),(c),(d),(e),(f) shows the switching modes of the proposed converter during T_s . Before $t = t_0$, S_2 and S_3 have been turned OFF. The voltages $V_{S\,1}$ and $V_{S\,4}$ have been zero when the primary current i_p flows through the body diodes $D_{S\,1}$ and $D_{S\,4}$.

III. Principle of Operation

Mode 1 [t_0, t_1]: At $t = t_0$, S_1 and S_4 are turned ON. Since $V_{Lm} = V_i$, the magnetizing inductor current i_{Lm} increases linearly as

$$i_{lm}(t) = i_{lm}(t_0) + \frac{V_i}{L_m}(t - t_0) \qquad (1)$$

At the secondary side, NV_i is applied to the secondary winding of T. The output diode $D_{o\,1}$ is turned ON. The series-resonant circuit consisting of L_{lk} and C_r is formed. By the series resonance between L_{lk} and C_r , the energy stored in C_r is transferred to C_o . The angular resonant frequency ω_r of the series-resonant circuit is

$$\omega_r = 2\pi f_r = \frac{1}{\sqrt{L_{lk} c_r}} \qquad (2)$$

Where f_r is the resonant frequency. By referring the output diode current i_{Do1} to the primary side, the primary current ip is expressed as

$$i_p(t) = i_p(t_0) + \frac{V_i}{L_m}(t - t_0) + N i_{D01}(t) \qquad (3)$$

Where the output diode current i_{Do1} is given by

$$i_{D01}(t) = \frac{V_0 - NV_i - V_r}{Z_r} \sin \omega_r (t - t_0) \qquad (4)$$

The resonant impedance Z_r is expressed as

$$Z_r = \sqrt{\frac{L_{lk}}{C_r}} \qquad (5)$$

Mode 2 [t_1, t_2]: At t = t_1, the half-resonant period of the series resonance is finished. The output diode current i_{Do1} is zero before $D_{o\,1}$ is turned OFF. $D_{o\,1}$ can be turned off at zero current without any diode reverse recovery current.

Mode 3 [t_2, t_3]: At t = t_2, S_1 and S_4 are turned OFF. The primary current i_p charges $C_{S\,1}$ and $C_{S\,4}$ and discharges $C_{S\,2}$ and $C_{S\,3}$. $V_{S\,1}$ and $V_{S\,4}$ increase from zero to V_i. $V_{S\,2}$ and $V_{S\,3}$ decrease from V_c to zero. Since the switch output capacitor C_S (= $C_{S\,1}$ = $C_{S\,2}$ = $C_{S\,3}$ = $C_{S\,4}$) is very small, the time interval during this mode is considered negligible compared to T_s.

Mode 4 [t_3, t_4]: At t = t_3, S_2 and S_3 are turned ON. Since $V_{Lm} = -V_c$, the magnetizing inductor current i_{Lm} decreases linearly as

$$i_{LM}(t) = i_{LM}(t_3) - \frac{V_c}{L_m}(t - t_3) \qquad (6)$$

At the secondary side, NV_c is reversely applied across the secondary winding of T. The output diode $D_{o\,2}$ is turned ON. The series-resonant circuit consisting of L_{lk} and C_r is formed again. The input power is transferred to C_r by the series resonance between L_{lk} and C_r. By referring the output diode current i_{Do2} to the primary side, the primary current i_p is expressed as

$$i_p(t) = i_p(t_3) - \frac{V_c}{L_m}(t - t_3) - N i_{D02}(t) \qquad (7)$$

Where the output diode current iDo2 is given by

$$i_{D02}(t) = \frac{NV_c + V_r}{Z_r} \sin \omega_r (t - t_3) \qquad (8)$$

Mode 5 [t_4, t_5]: At t = t_4, the half-resonant period of the series resonance is finished. The output diode current i_{Do2} is zero before $D_{o\,2}$ is turned OFF. $D_{o\,2}$ can be turned OFF without any diode reverse-recovery current.

Mode 6 [t_5, t_6]: At t = t_5 , S_2 and S_3 are turned OFF. The primary current i_p charges $C_{S\,2}$ and $C_{S\,3}$ and discharges $C_{S\,1}$ and $C_{S\,4}$. $V_{S\,2}$ and $V_{S\,3}$ increase from zero to V_c. $V_{S\,1}$ and $V_{S\,4}$ decrease from V_i to zero. Since the capacitor C_S is very small, the time interval during this mode is considered negligible compared to T_s. The next switching cycle begins when S_1 and S_4 are turned ON again.By the voltage-second balance relation on the magnetizing inductor L_m, the voltages V_c and V_r are expressed as

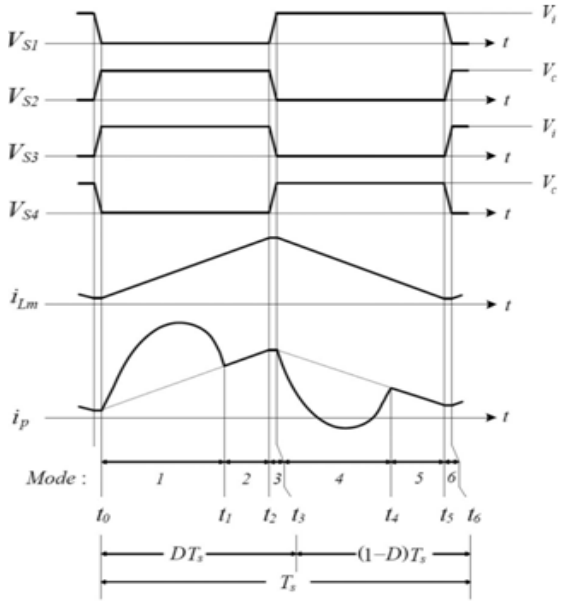

Fig.2 switching waveforms of proposed converter

$$V_c = \frac{D}{1-D} V_i \qquad (9)$$

$$V_r = (1-D)V_0 \qquad (10)$$

For the voltage-second balance relation on the secondary winding of T during T_s , the following relation between the output voltage V_o and the input voltage V_i is obtained as

$$\frac{V_0}{V_i} = \frac{N}{1-D} \qquad (11)$$

The maximum voltage stress of S_1 and S_3 is confined to the input voltage V_i . The voltage stress of S_2 and S_4 is confined to the clamping capacitor voltage V_c. The relation between the clamping capacitor voltage V_c and the duty ratio D. The dual active-clamping circuit is used in the proposed converter. The clamping capacitor voltage in case of the dual active-clamping circuit is always lower than the clamping capacitor voltage in case of the conventional active-clamping circuit. It means that the switch voltage stress of the proposed converter is always lower than the switch voltage stress of the previous converter using the conventional active-clamping circuit. Especially, when the duty ratio is below 0.5, the clamping capacitor voltage can be lower than the input voltage V_i. It is critically beneficial in low-voltage PV applications where more than 50% of the power losses are lost as switching power losses.

The output diode currents i_{Do1} and i_{Do2} should be zero before the output diodes $D_{o\,1}$ and $D_{o\,2}$ are turned OFF. The half-resonant period of the series resonance during Mode 1 and Mode 4 should be finished before the output diode is turned OFF. The following condition should be satisfied for zero-current turn-off of the output diode as

$$\sin[\omega_c D_{max} T_s] = 0, \quad \text{if } D_{max} \le 0.5 \qquad (12)$$

$$\sin[\omega_r (1 - D_{max}) T_s] = 0, \quad \text{if } Dmax > 0.5 \qquad (13)$$

Where D_{max} is the maximum duty ratio. ω_c is the critical angular resonant frequency as $\omega_c = 2\pi f_c$. f_c is the critical resonant frequency of the series-resonant circuit. For zero-current turnoff of the output diode, the resonant frequency f_r should be higher than the critical resonant frequency f_c . Then, the resonant capacitor C_r should be determined as

$$C_r < \frac{1}{\omega_c^2 L_{lk}} = \frac{D_{max}^2 T_s^2}{\pi^2 L_{lk}}, \quad \text{if} \quad D_{max} \le 0.5 \qquad (14)$$

$$= \frac{(1-D_{max})^2 T_s^2}{\pi^2 L_{lk}}, \quad \text{if} \quad D_{max} > 0.5 \qquad (15)$$

IV. Experimental Results

The proposed converter has been built to verify its performance with the following parameters:

1) input voltage, V_i : 50–60 V;
2) output voltage, V_o : 550 V;
3) output power, P_o : 450 W;
4) switching frequency, f_s : 50 kHz;
5) input capacitor, C_i : 13.2 mF;
6) clamping capacitor, C_c : 680 μF;
7) switch output capacitor, C_S : 500 pF;
8) transformer turns ratio, N: 4;
9) magnetizing inductor, L_m : 9 μH;
10) leakage inductor, L_{lk} : 3 μH;

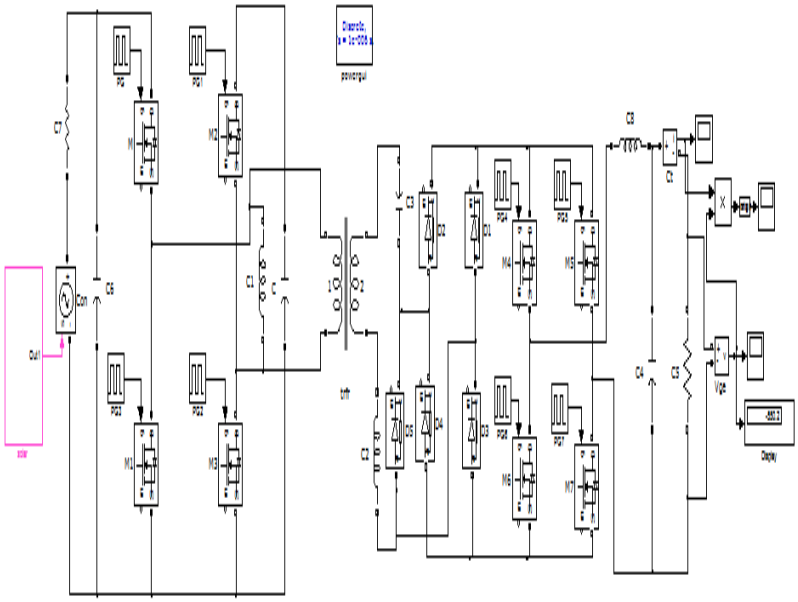

Fig.3 Simulation circuit diagram of the proposed converter

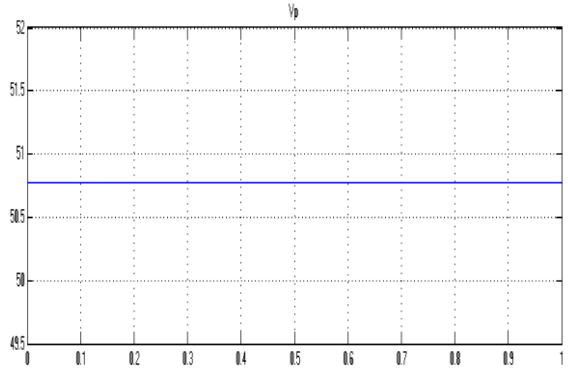

Fig.4 Input voltage

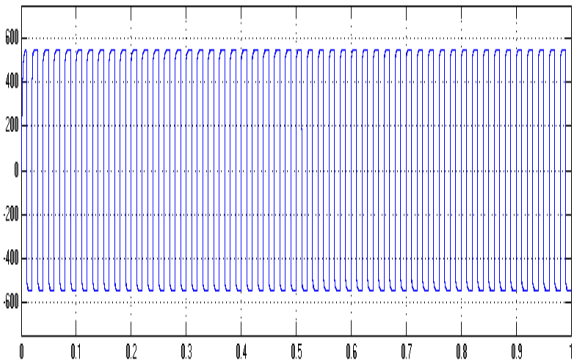

Fig.5 Output voltage

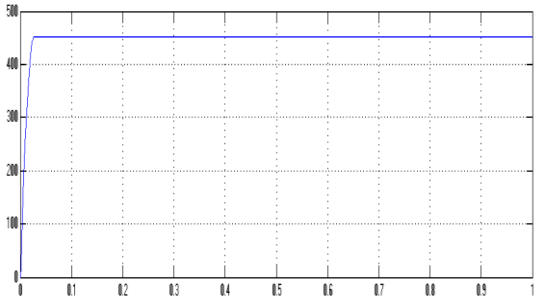

Fig.6 Output power

V. Conclusion

This paper has presented the procedures for the capacity and controller design of the high-efficiency dc–dc converter with fast dynamic response for low-voltage PV sources. The operation of the proposed converter has been described. Full bridge converter is used to increase the output voltage. Π filter is used to reduce ripples in the output. The dynamic response of the proposed converter is improved. The simulation circuits are developed using elements of simulink library. The Simulation is successfully done and open loop / closed loop simulation results are presented.

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